Automotive Safety and Convenience Data Book 1995

TEMIC

TELEFUNKEN Semiconductors

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Introduction

In the present age of modern communication and increasing mobility, there is an increasing demand for remote control systems. Reasons for using wireless systems are numerous and can not only be for comfort, versatility and flexibility but also for safety and cost savings. This is valid for various applications, such as keyless entry systems for cars and buildings, alarm and security systems, domestic installations and wireless data transfer systems. Wireless data transmission, that means IR- as well as RF-based systems, is well-suited to supply the customer's needs for safety and convenience.

TEMIC is working more than 20 years in the area of remote control. With this experience, we can offer our customers dedicated ICs for infrared remote control as well as for radio frequency systems.

Keyless Entry

The remote keyless entry (RF or IR) replaces the traditional key and is either incorporated in the key chain or mechanically integrated in the key. Small size is a must for remote keyless entry. By offering complete chip sets for compact system solutions and complete transmitter micromodules in chip-on-board technique, the necessary miniaturization can be realized.

The TEMIC 4-bit microcontroller family is suitable to encode/ decode the transmission code as well as to control the central door lock.

Immobilizer

A new security system for cars is the electronic immobilizer with an integrated microtransponder in the key. This system requests for an individual identification by the owner of the car. Only if this identification, located in the key, matches with the identifier in the car, the engine functions are enabled.

The complete reader functions are integrated in TEMIC's reader IC, arranged round the ignition lock. It can be used along with TEMIC's transponder and the 4-bit microcontroller family to create a complete, compact and effective anti-theft system with a minimum of components.

MARC4 Family

The TEMIC MARC4 microcontroller family bases on a low-power 4-bit CPU core, the modular architecture is HARVARD-like. This µC family is well-suited for keyless entry- and immobilizer applications as an encoder/ decoder (RF- and IR-systems).

1. Keyless Entry

The U431xB IC family is designed to realize a low-current UHF remote control system. This system is flexible with regard to amplitude or frequency modulation, different transmission coding and a wide range of data rates. The transmitter as well as the receiver are likewise equipped with a surface acoustic wave (SAW) resonator for purpose of frequency stabilization.

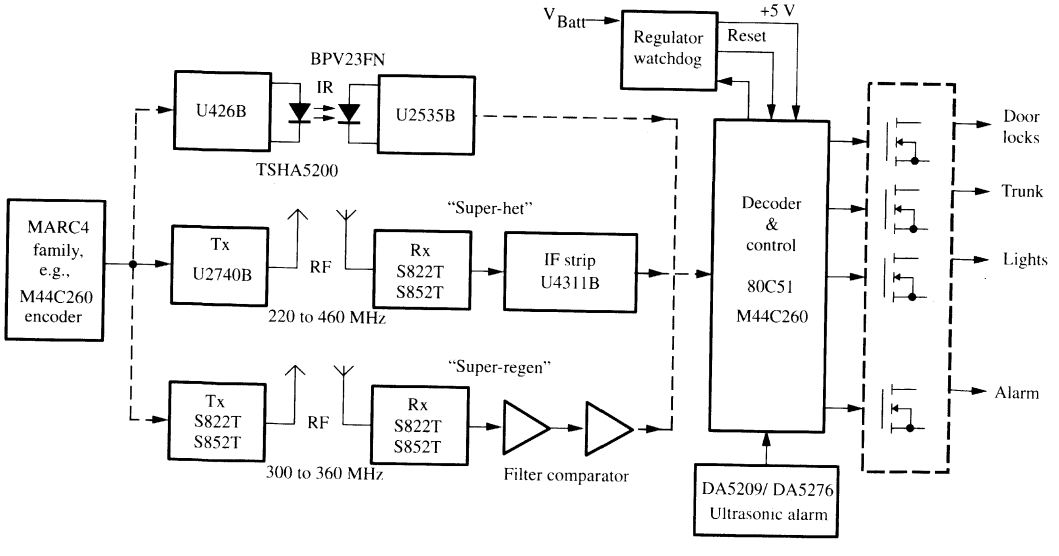
For both, the transmitter and the transceiver's front end, the UHF transistors S822T/ S852T are used, as they are well-suited for low-current operation. The superheterodyne receiver is based on one of the receiver ICs U4311B/ U4313B of TEMIC.

These monolithic ICs in bipolar technology include all necessary parts from IF signal processing to data output. The receiver ICs, together with the transistors and the low-power microcontroller M44C260, make it possible to realize an UHF receiver with an average current consumption of approximately 1 mA. This out-standing feature is achieved by a standby- or a polling concept in conjunction with a special circuit arrangement.

A further type of receiver ICs is the U4314B, which is suited exclusively for AM operation. It achieves a supply current below 1 mA without any sleep mode, but also without baseband processing.

The U2740B is a single-chip PLL transmitter for automotive keyless entry. With an on-board voltage-controlled oscillator (VCO), the U2740B provides a compact solution for small form-factor designs with improved performance over SAW-based transmitters.

System Solution for Keyless Entry



Comparison Infrared versus RF-Systems

The infrared key for remote controlling of central locking systems in cars is now a standard feature of luxury- and mid-range cars. It will also be offered in the lower vehicle ranges in the near future. IR remote control systems are inexpensive, well experienced and can be easily realized with conventional production techniques. Recently in some areas, low-power radio links are replacing infrared systems. Especially in the car market, RF-based systems offer the advantage of not being affected by dirt, ice and snow. Nowadays, the car's windows are often additionally shaded to reduce excessive heating of the car interior. Unfortunately, the shading attenuates the IR transmission of the remote control systems just as much as the emission from the sun.

If we compare the advantages and drawbacks of infrared and radio frequency systems, it becomes obvious that radio frequency technology helps to overcome some of the restrictions of infrared technology. However, in the infrared technology are other problems to be solved; so both systems are likely to co-exist.

The Infrared System

Common infrared remote control systems use a gallium-arsenide light-emitting diode as transmitter which emits light of 800 nm to 1000 nm wavelength. It is possible to speak of rectilinear propagation. Reflection mainly takes place at visibly reflecting surfaces. Diffraction at edges is restricted to just a few wavelengths and can therefore be neglected. For this reason, several receiving diodes should be installed to ensure correct operation under various conditions. If appropriate, an omni-directional receiving diode can be used. Operation of the system is restricted to an area in which the user can see the reaction. Interference may be caused by continuous light from the sun and from the headlights of other vehicles, 100 Hz components of mains-operated incandescent lamps and their harmonics in the case of gas-discharge lamps. Recently, interfering light in the 30-kHz band from modern energy-saving lamps with switched-mode power supply also has to be considered. Spectral components of the data signal within these frequency bands should be avoided by coding.
On the transmitter side, for purpose of current saving, pulse position modulation with an extremely low mark-to-space ratio is used. Operation is done by a single IRED (**I**nfra **R**ed **E**mitting **D**iode) with an extreme directional characteristic. This high directional characteristic of the IRED is a frequent object of customer criticism, since aiming at the target with the key is not accepted.
If we are looking at the receiver, the infrared system is quite simple. A photodiode converts the received light into a current which can then be converted into digital signals by special circuits without a high-power requirement. Higher system costs may result from the use of several receiving diodes due to the increased expense of installation. The costs for the subassemblies of the IR system however will always be low, compared to the RF system.

The RF-System

RF systems operating in the UHF band are not restricted to the line-of-sight coverage of optical systems due to diffraction and reflection of radio waves at edges and conductive surfaces as well as their capability to penetrate dielectric materials. This becomes apparent in an even illumination of space under complicated spatial circumstances as in buildings. Also the necessity to aim with the transmitter at the receiver is removed, because the commonly used small, low-gain aerials show an almost perfect omni-directional radiation pattern. The range of the RF system can not be well defined because of the mentioned propagation characteristic and due to additional polarization losses. These may vary from zero up to approximately 20 dB, depending on the relative orientation of the transmitter and the receiver antennas. Nevertheless in most cases, there is a high statistical probability of sufficient field strength.
One the other side, a problem could be the probability of excess range, such as when several conductive surfaces are coincidentally located close to the transmitter or receiver in a way that they form the elements of a parabolic reflector. Wave guidance occurring along conductive planes, for instance in a multi-storey car park, may increase the operation range as well. In this case, a considerable discrepancy between the optical perception range of the user and the range of the transmission link exists. For applications with higher security claims, misuse must be prevented. Listening-in to the radio frequencies with sensitive special receivers appears to be a problem. Average technically-orientated criminal intelligence is sufficient to receive, store and re-transmit a data telegram without changing code. These problems were mentioned before when infrared transmission links were introduced, but seemed to be not critical owing to the restricted range and directional effect of the IRED.

Dedicated ICs for Keyless Entry/ Remote Control

Product	Function	Key Features	Benefits
IR-remote control/ keyless entry			
U2535B-FP	IR preamplifier	f = 20 to 100 kHz; I = typ. 260 µA at 12 V	Lowest power consumption
U2538B-FP	IR preamplifier	AGC; I = typ. 500 µA at 5 V	Wide transmission distance
U426B-FP	IR driver, transmitter	I = 0.2 to 1.2 A; f up to 500 kHz	Universal IRED-driver
RF-remote control/ keyless entry			
U4311B U4311B-FL	UHF receiver, 10.7 MHz, IF amplifier, data filter, and data shaper, log. RSS	AM+FM demodulator, non-inverting clamping comparator	Low-power consumption, typ. 1.0 mA, complete IF- and baseband processing
U4313B U4313B-FL		AM+FM demodulator, inverting clamping comparator	Low-power consumption, typ. 1.0 mA, complete IF- and baseband processing
U4314B-FP	UHF receiver, 10.7 MHz IF amplifier., log. RSSI	AM demodulator, RF-level indicator	Low-power consumption, typ. 0.8 mA
U2740B	UHF AM/FM transmitter	Wide frequency range (200 to 500 MHz), output level control	Increased system performance, compared to SAW-based transmitters: enlarged FM deviation and reduced costs; possibility to use PLL-Ref. XTAL for µC

Microcontrollers: see chapter 3

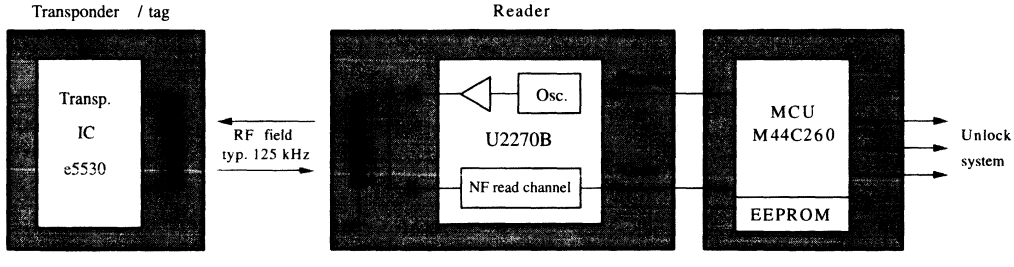
2. Immobilizer

The last years, increasing car theft statistics have shown more and more the urgency for protection. Since 1995, car insurances demand that new cars have to be protected against theft by an immobilizer.

An immobilizer is a passive theft protection, that means, the transponder needs no battery but is supplied via the reader. Therefore, the immobilizer offers best safety and reliability in operation.

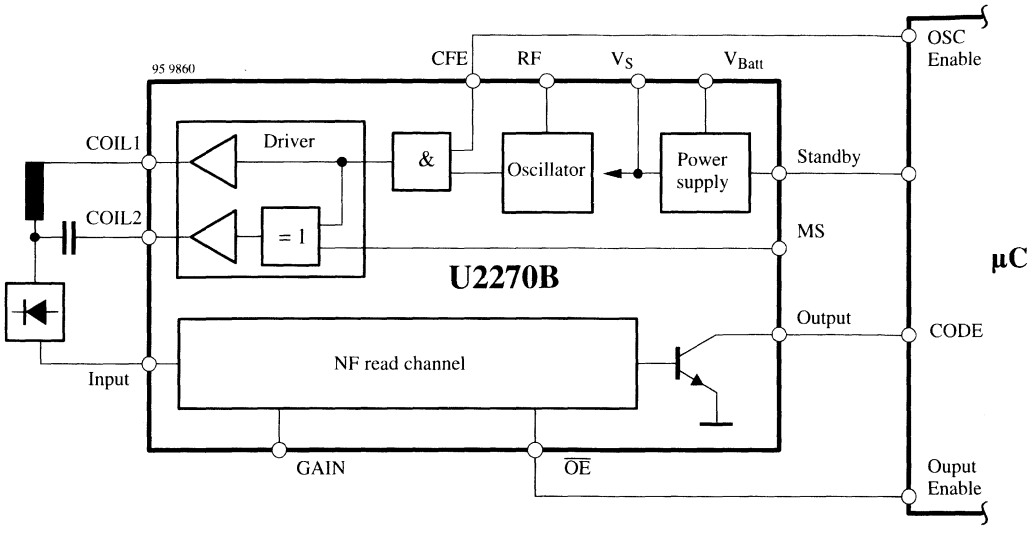
The industry's first single-chip reader IC for automotive immobilizer anti-theft systems was released by TEMIC in November 1994. The U2270B combines flexible reader coil driver circuitry, a highly integrated NF read-channel and an on-chip power supply. Along with TEMIC's e5530 transponder and M44C260 micro-controller, the U2270B can be used to create a complete, compact and effective anti-theft system with a minimum of components.

System Solution for Immobilizer



- Contactless readout of up to 128 bit unique identifier
- Power supply via RF field
- AM modulation by damping the magnetic field by the code
- Tuneable oscillator to optimize the magnetic coupling
- Flexible driver suitable for all kind of antennas
- NF read channel with µC-compatible output
- The demodulated code is compared with the identifier in the EEPROM
- System is only unlocked if codes are matching

Reader IC U2270B



The U2270B serves as interface between the transponder and the microcontroller that compares the received data. This interface operates bidirectional.

One direction is the energy transfer from the reader to the transponder. The reader creates a magnetic field via a reader air coil. This coil is operated by a special driver circuit. The driver consists of two output stages that can be operated in common or in differential mode via the pin MS. Using this feature, the user is flexible in the design of the antenna. The driver is controlled by an on-chip oscillator. The operating frequency is programmed by an external resistor. This enables the user to externally adjust the frequency to the relevant circumstances. This feature is important to compensate frequency tolerances of the antenna and the transponder. The oscillator can be disabled through pin CFE to enable read-write operation.

The other direction is the data transfer from the transponder to the microcontroller. The transponder modulates the magnetic field with its internal data. This leads to a tiny voltage modulation at the reader coil. Via a rectifier, this signal is fed into the input pin of the reader IC. The NF read channel amplifies and conditions the signal to convert it to the appropriate digital output data. The gain of the amplifier can be programmed through pin GAIN to adopt to the relevant reading distance. An open collector output serves as interface to the connected controller. With a logic signal at pin OE, the data output can be disabled.

The reader IC also incorporates an internal power supply. This enables the user to operate the system from a 12-V supply but also from an existing 5-V supply rail. Via the pin Standby, the U2270B can be set to a power-down mode where the supply current is very low.

Dedicated ICs for Immobilizer

Product	Function	Key Features	Benefits
U2270B-FP	Reader IC	RF generator, coil driver, filtering-on-chip	Suitable for R/W- and read-only systems
e5530*	Transponder	Contactless operation	Read-only operation
e5550**	Transponder	Read/ write (Q3/95)	
e5560**	Transponder	Read/ write, encryption key (in development, Q1/96)	

Microcontroller: see chapter 3

Note: * = Available in GT (glass tube) and PC (plastic case); PC is in development (Q4/95)
** = Available in PC (plastic case), PC is in development (Q4/95)

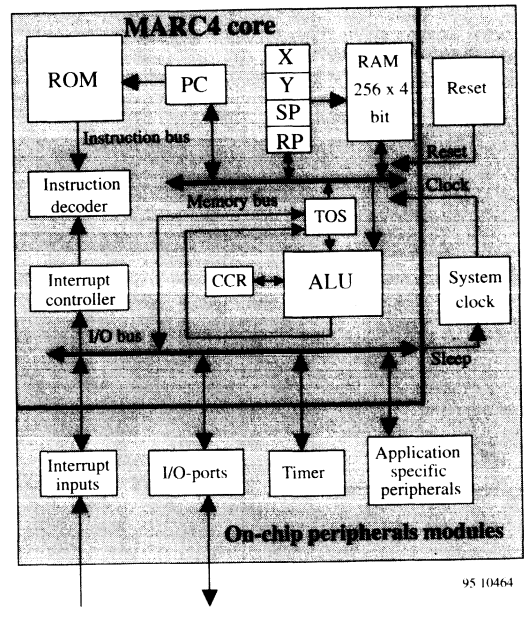
3. MARC4 Microcontroller Family

The TEMIC MARC4 microcontroller family bases on a low-power 4-bit CPU core. The modular MARC4 architecture is HARVARD-like, high-level language oriented and well-suitable to realize high integrated microcontrollers with a variety of application- or customer-specific on-chip peripheral combinations. The MARC4 controller's low voltage and low-power consumption is perfect for hand-held and battery-operated operations. The standard members of the family have selected peripheral combinations for a broad range of applications.

Programming is supported by an easy-to-use PC-based Software Development System with a high-level language qFORTH compiler and an emulator board. The FORTH-oriented microcontroller conception enables the qFORTH compiler to generate a very compact and efficient MARC4 program code.

Features

- 4-bit HARVARD architecture
- High-level language oriented CPU conception
- Three-stage pipeline structure
- 256 × 4 nibbles of RAM
- Up to 9 kBytes of ROM
- Eight vectored prioritized interrupt levels
- Low-voltage operation range
- Low-power consumption
- Power-down mode
- Various on-chip peripheral combinations available
- High-level language programming in qFORTH
- Programming and testing support by an integrated Software Development System



Dedicated ICs for Microcontrollers

Product	Function	Key Features	Benefits	Availability
M43C200	4-bit MCU	10 I/O, 4 IN, 3 interrupts	Low standby current (3 modes), SO 24	Now
M43C201	4-bit MCU	8 I/O, 2 IN, 2 interrupts	Low standby current (3 modes), SO 16 L	Now
M44C260	4-bit MCU	128-bit EEPROM, 2 timers	Optimized for remote control; low power, low current (1 µA)	Q3/95
M48C260	4-bit MCU, EEPROM instead of ROM	User-programmable M44C260	Re-programmable, program memory	Q3/95

General Information

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Preamplifier for IR Remote Control

Description

The IC U2535B-FP is a complete IR receiver for data communication. The PIN-photodiode converts the transmitted IR-telegram into the electronic input signals. This is separated by a special input circuit. The characteristics (filter, gain) of the following amplifier is determined by external components. The signal detector, consisting of a comparator, an integrator and a Schmitt trigger, forms the input signal to an output pulse that can be interfaced to a microcomputer.

Features

- Low current requirement (typical 260 µA/ 12 V)
- Carrier frequencies between 20 to 100 kHz
- Supply voltages: 5 or 7 to 16 V with internal stabilisation
- Filter characteristics and gain are specified by few external components
- Demodulator with Schmitt-trigger
- Open collector output

Applications

- Keyless entry
- Remote control
- Wireless data transfer

Case: SO8

Block Diagram

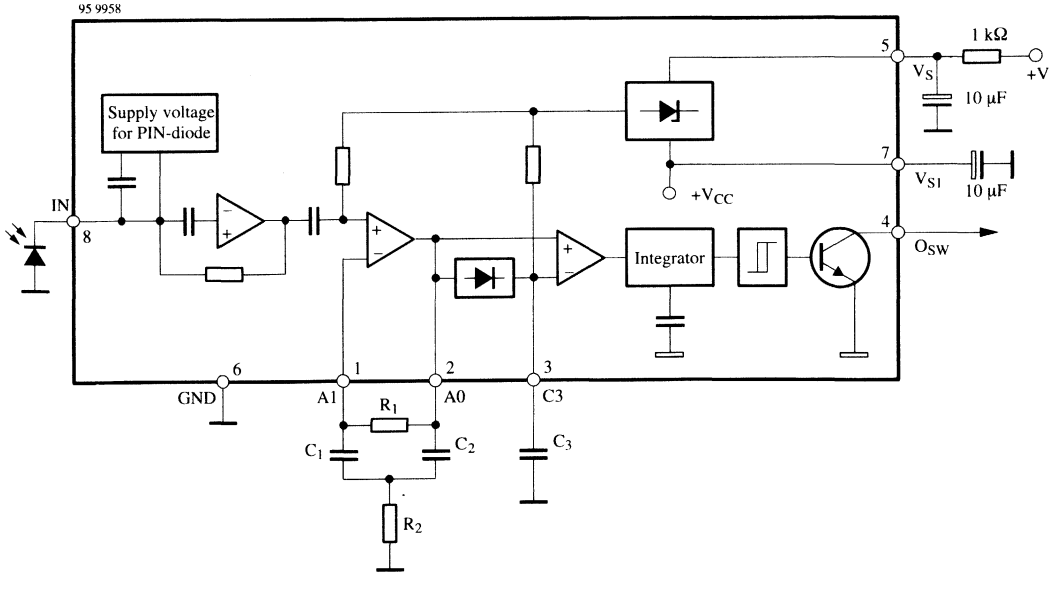
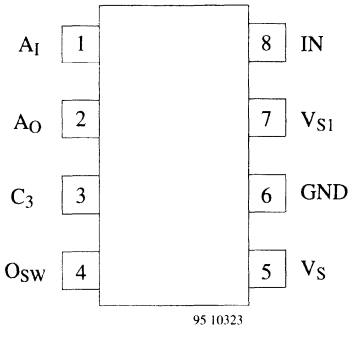


Figure 1. Block diagram

Pin Description



Pin	Symbol	Function
1	A_I	Inverting input of band pass amplifier, pin connection for external filter function
2	A_O	Output of band pass amplifier
3	C_3	Capacitor at Pin 3 to reject (suppress) ripple during transmission, also functions as delay time for reference voltage of the comparator
4	O_{SW}	Switching output It is an open collector output which switches with time delay and goes LOW (transistor switched ON), when the signal is identified at Pin 2.
5	V_S	Supply voltage The integrated Z-diode (typical 17 V) protects the circuit against positive voltage spikes
6	GND	Ground
7	V_{S1}	Unregulated supply voltage for 5 V operation
8	IN	Input connection for photodiode with regulated bias voltage

Absolute Maximum Ratings

Reference point Pin 6, unless otherwise specified

Parameters		Symbol	Value	Unit
Supply voltage range	Pin 5	V_S	–0.3 to +16	V
Supply currents:	Pin 5	I_S	20	mA
$tp \leq 250$ ms	Pin 5	i_S	150	mA
Input voltages	Pin 1	$V_{A(I)}$	–0.3 to 5	V
	Pin 4	$V_{0(SW)}$	–0.3 to 16	V
	Pin 8	V_{IN}	–0.3 to 5	V
Output currents	Pins 2 and 4	I_0	±5	mA
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	–40 to +125	°C
Ambient temperature range		T_{amb}	–40 to +105	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	180	K/W

Electrical Characteristics

T_{amb} = 25°C, reference point Pin 6, test circuit, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply currents	V_{S1} = 5 V, I_{IN} = 0, Pin 7 V_S = 12 V, I_{IN} =0, Pin 5	I_{S1} I_S	140 200		200 320	µA µA
Internal stabilisation	V_S = 12 V, I_{IN} = 0, Pin 7	V_{S1}	4.9		5.4	V
Maximum input current	V_{S1} = 5 V, V_{IN} = 0, Pin 8	$-I_{IN}$	0.8		1.2	mA
Low level voltage	V_{S1} = 5 V, I_{OL} = 0.5 mA Pin 4	V_{OL}			0.2	V
Leakage current	V_{S1} = 5 V, V_0 = 12 V, Pin 4	I_{OH}			1	µA
Input stage, amplifier						
Cut-off frequency		f_L f_H	 100		15	kHz kHz
Gain	v_i = 2 mV_{rms}, f = 40 kHz f = 100 kHz	 G_v G_v	 47 46	 50 49		 dB dB
Detector						
Threshold voltage	$t_d \leq 200$ µs, f = 40 kHz, Pin 2	V_{A0}		150		mV_{rms}
Delay time	f = 40 kHz, V_{A0} = 1 V_{rms} see figure 3	t_d	50	90		µs
Storage time	f = 40 kHz, V_{A0} = 1 V_{rms} see figure 3	t_s	100		150	µs

Test Circuit

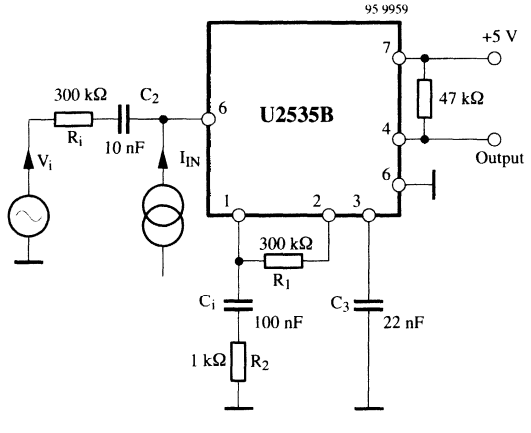


Figure 2.

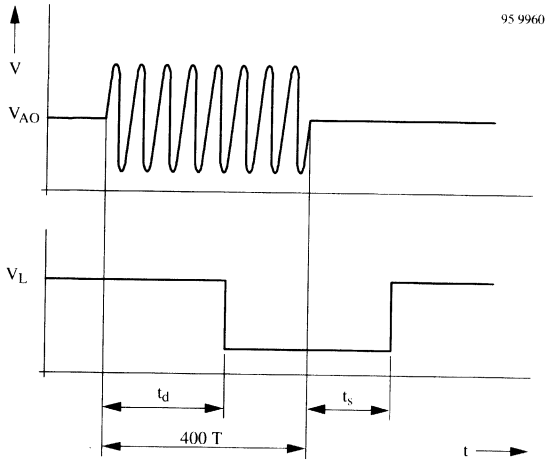


Figure 3.

Application Circuit

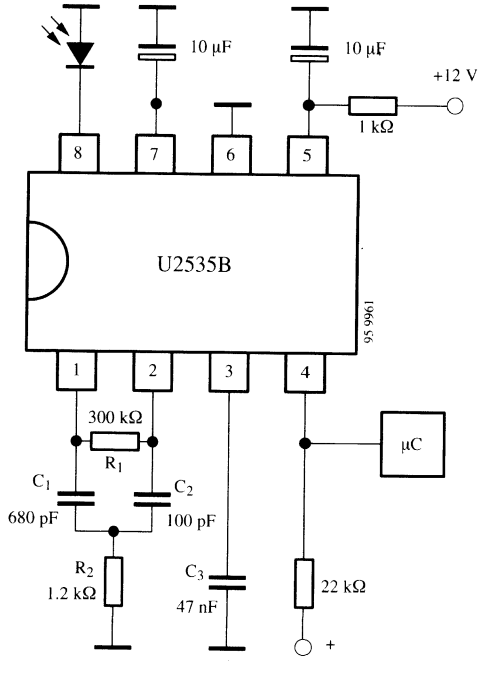


Figure 4.

Band Pass Filter Design

Center frequency

$$f_O = \frac{1}{2\pi \sqrt{R_1 \times C_1 \times R_2 \times C_2}}$$

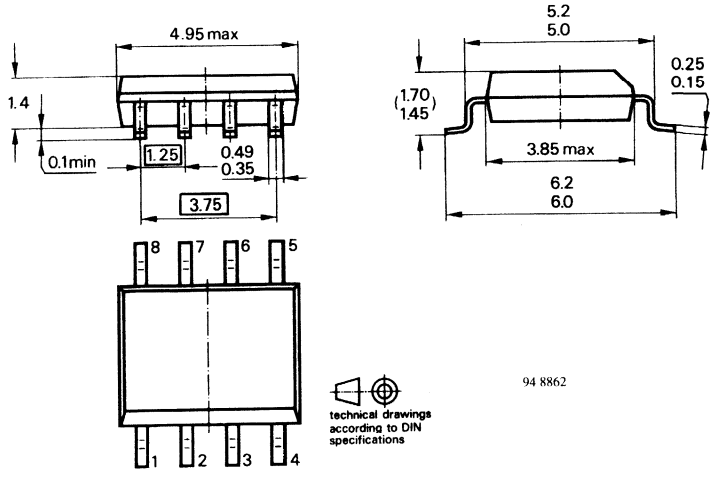
$$GAIN \approx \frac{R_1 \times C_1}{R_2 (C_1 + C_2)} \qquad R_1 >> R_2,\ C_1 \geqq C_2$$

$$Bandwidth \approx \frac{C_1 + C_2}{2\pi \times R_1 \times C_1 \times C_2} \qquad BW << f_O$$

Note: R_1 should be about 300 kΩ.
Results can be influenced by feedback (Pin 2 → Pin 8)

Dimensions in mm

Package: SO 8



U2538B

IR Receiver for Data Communication

Description

The IC U2538B is a complete IR receiver for data communication. The useful input signals are separated by a special input circuit and amplified by a gain-controlled amplifier. The bandpass filter suppresses the off-band signals. The signal detector, consisting of a demodulator, an integrator and a Schmitt Trigger, forms the input signal to an output pulse that can be interfaced to a microcomputer. The AGC and the ATC circuit control the receiver's sensitivity, making it insensitive to ambient light sources.

Features

- Few external components
- Low power consumption
- Microcomputer compatible
- Insensitive to ambient light and other continuous interference

Applications

- Keyless entry systems
- Remote control
- Wireless data transfer up to 4 kbit/s

Case: SO8 U2538B-FP

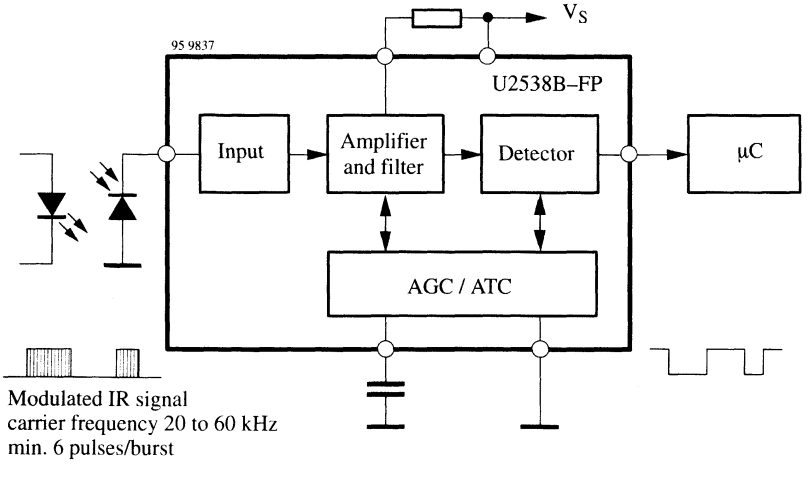


Figure 1.

Pinning

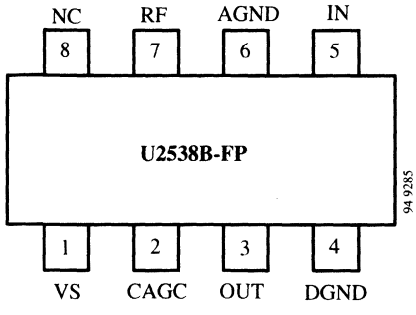


Figure 2.

Pin Description

Pin	Symbol	Function
1	VS	Supply voltage
2	CAGC	AGC capacitor
3	OUT	Data output
4	DGND	GND – DEM/INT/ST
5	IN	Input pin diode
6	AGND	GND amplifier
7	RF	Frequency determination
8	NC	Not connected

Block Diagram

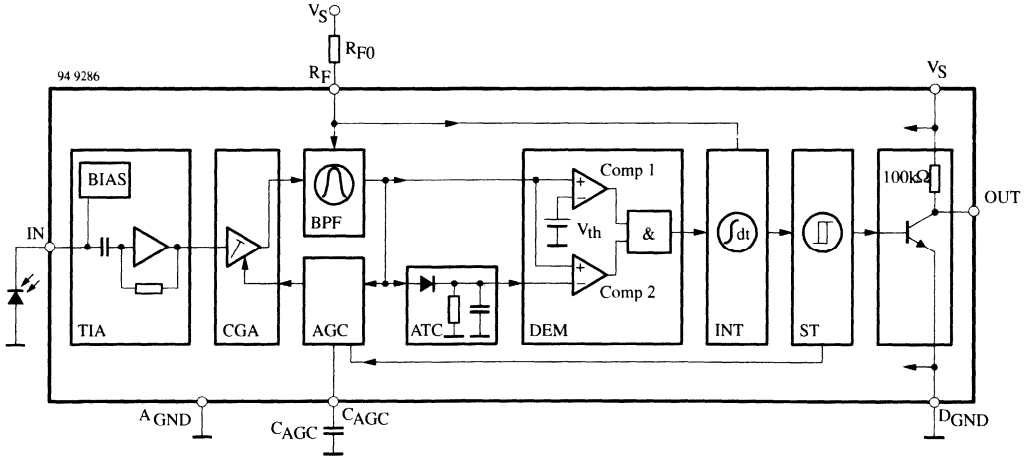


Figure 3.

TIA Trans impedance amplifier
CGA Controlled-gain amplifier
BPF Bandpass filter
AGC Automatic gain control
ATC Automatic threshold control
DEM Demodulator
INT Integrator
ST Schmitt Trigger

Functional Description

Input Stage (TIA)

The input stage provides the necessary bias voltage for the photo diode and ensures decoupling of the useful signal. This involves processing the dc and ac portions in separate parts of the circuit: the bias voltage (BIAS) and the transimpedance amplifier circuit (TIA). The bias voltage circuit operates like a load resistor with respect to the photo diode, the value of which is low for dc and low-frequency signals (3 to 100 kΩ) but as high as possible for the operating frequency (100 kΩ to 1 MΩ) depending on the input current) The ac portion of the input signal feeds an inverted amplifier with a sufficiently low input resistance (Z_i < 10 kΩ). If the input resistance were too high, the useful signal would be lost to the junction capacitance of the photo diode.

Gain Controlled Amplifier (CGA)

The gain controlled amplifier accounts for the greatest part of the voltage gain and can be controlled via the voltage at C_{AGC} (pin 2). Gain control is needed to support the interference suppression of the detector. High-pass behaviour results from the capacitive coupling of the individual stages. The cut-off frequency is approximately 20 kHz.

Bandpass Filter (BPF)

The bandpass filter is largely made up of integrated components. An external resistor determines the mid-frequency. The filter quality is about 7 and is practically independent of the selected mid-frequency (see figure 4). The following formula can be used for calculating the resistor, R_{f0}:

$$R_{fO}\ (k\Omega) = \frac{8855}{f_0\ (kHz)} - 13$$

where: 20 kHz < f_0 < 60 kHz

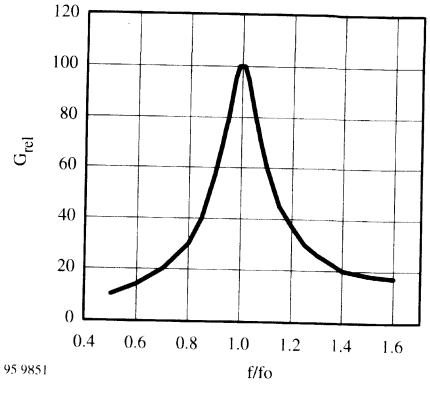


Figure 4. Characteristic of the bandpass filter

Automatic Threshold Control (ATC)

During the reception of an incoming telegram, the ATC reduces the sensitivity of the demodulator to establish the highest possible signal to noise ratio according to the signal strength. This prevents interferences, which may arise during the transmission from affecting the output. The advantage of the circuit is attained, if its output voltage exceeds V_{Th} (Comp 1). That is the case, when the input signal strength is more than double of the minimum detectable signal intensity.

Automatic Gain Control (AGC)

The automatic gain control improves the circuit's resistance to interference by adapting the amplification of the gain controlled amplifier to the relevant existing interference level. In order to prevent the circuit from responding to transmitted data signals, it gradually reduces the sensitivity but only if the duty cycle exceeds a specific value (see figure 5). When using telegrams with higher duty cycles than this value, the capacitor, C_{AGC}, maintains the sensitivity for a certain time period. A higher cpacitance enables a longer transmission time. A capacitance of C1 = 22 nF is adequate for most known telegrams. A typical value for the maximum duty cycle (DC) can be calculated by the following formula:

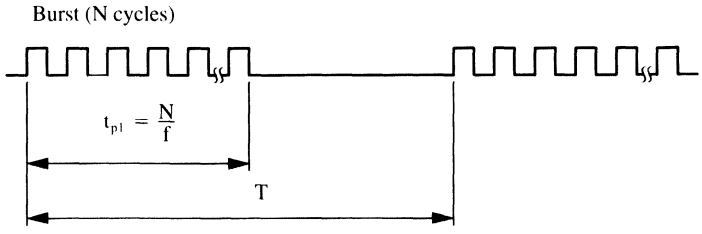


Figure 5.

Detector

The output signal of the bandpass filter is compared to a fixed reference (Comp 1) and to a reference generated by the ATC circuit (Comp 2). The output of the comparator with the higher threshold voltage controls the integrator. Use of the integrator keeps the output free of short-time interference.

The integrator drives the output stage after being processed through a Schmitt Trigger. The internal pull-up resistor can replace an external resistor, in some applications.

$$DC_{max} = \frac{N}{14.2 + 1.1\ N}$$

Absolute Maximum Ratings

Parameters		Symbol	Value	Unit
Supply voltage	Pin 1	V_S	–0.3 to +6.0	V
Input voltages	Pins 2, 3 and 5	V_{IN}	–0.3 to V_S	V
	Pin 7		–0.3 to +1.5	
Input current	Pin 7	I_{IN}	0 to 0.1	mA
Power dissipation	T_{amb} = 105°C	Ptot	110	mW
Junction temperature		Tj	125	°C
Ambient temperature		T_{amb}	–40 to +105	°C
Storage temperature		T_{stg}	–40 to +125	°C

Maximum Thermal Resistance

Parameters	Symbol	Maximum	Unit
Junction ambient	R_{thJA}	180	K/W

Electrical Characteristics

T_{amb} = 25°C, V_S = 5 V

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 1	V_S	4.5		5.5	V
Supply current	Pin 1	I_S	0.35		0.65	mA
Max. input current V_{IN} = 0	Pin 5	I_{IN}	0.6			mA
Output voltage low: I_{OL} = 2 mA	Pin 3	V_{OL}			0.2	V
Internal pull up resistor	Pin 3	R_L	75	100	125	kΩ
Center frequency of bandpass RF = 240 k		f_0	33.3	35	36.7	kHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Q factor		Q		7		
Freqency range		f	20		60	kHz
AGC current source sink	Pin 2		90 70	120 100	155 140	nA nA
AGC slope	Pin 2			20		dB/V
Nr. of pulses required			6			
Sensitivity	Pin 5				0.7	nA(rms)
Switch on delay, i_{IN} = 0.7 nA (rms)	Pin 3 see figure 6	t_{don}	3		7.5	Period
Switch off delay, i_{IN} = 0.7 nA (rms)	Pin 3 see figure 6	t_{doff}	5		10	Period
Pulse width, i_{IN} = 0.7 nA (rms), 6 pulse burst	Pin 3 see figure 6	t_{po}	4.5		10	Period

$$R_{fO}\ (k\Omega) = \frac{8855}{f_0\ (kHz)} - 13\ k\Omega$$

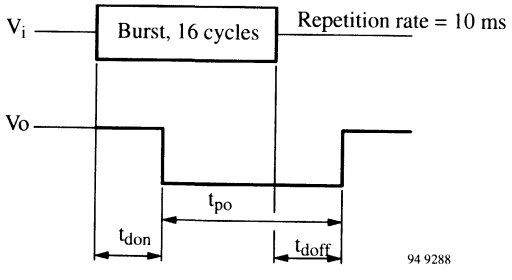
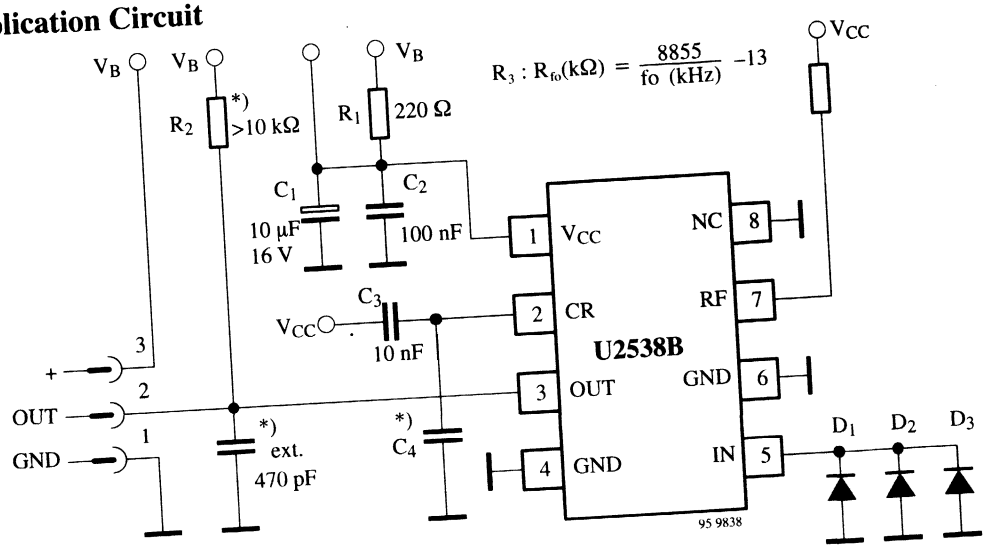


Figure 6.

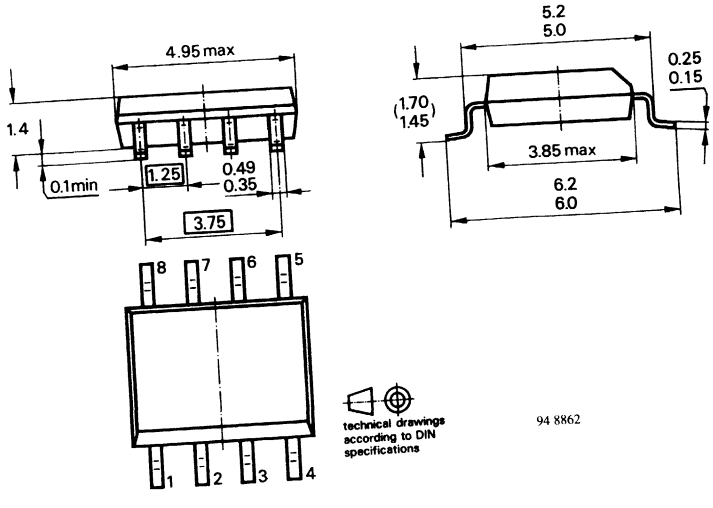
Application Circuit



*) optional: feedback reduction

Dimensions in mm

Package: SO 8



U2740B

UHF AM/FM Transmitter

Description

The U2740B is a one-chip multi-purpose UHF AM/FM transmitter designed for various applications in a wide frequency range. When supplying a **C**hip-**S**elect signal (CS), the IC starts operation (Power-up, XTO, VCO, PD) and the VCO is then locked to 128*f(XTO). The locked status is indicated by the **L**ock-**D**etect (LD) output.

The digital data is supplied to either an AM- or FM-input-pin whereby the output power is set by use of the AM-input-pin. A differential output provides simple application with loop antennas. An output driver (XTO out) can be used for clocking the microcontrolller.

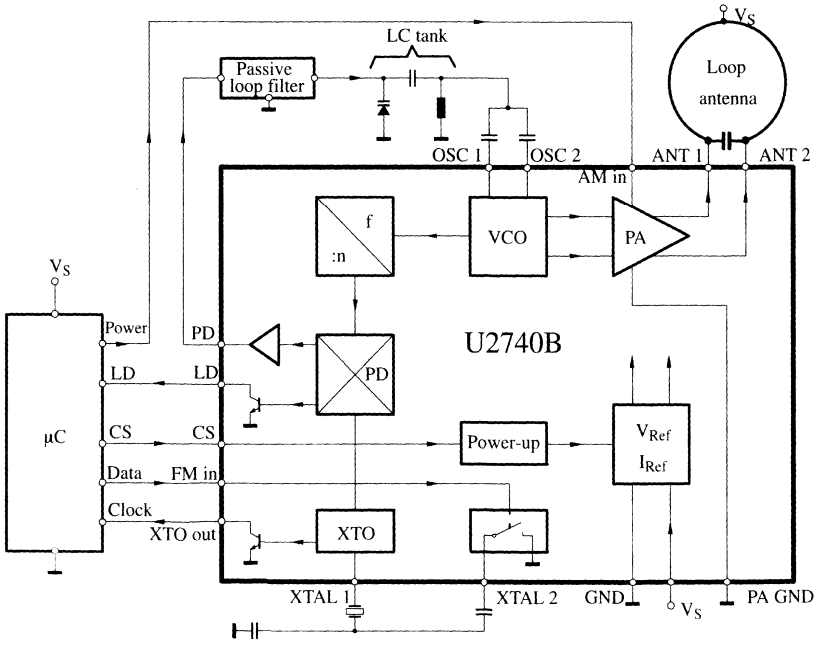
Features

- One-chip solution with few external components
- Wide frequency range (200 to 500 MHz)
- Single voltage supply (2.4 to 6 V) with power down feature
- Adjustable output power with differential output for loop antenna
- PLL lock-detect signal
- XTO output for µC clock
- ESD protection according to MIL-STD. 883

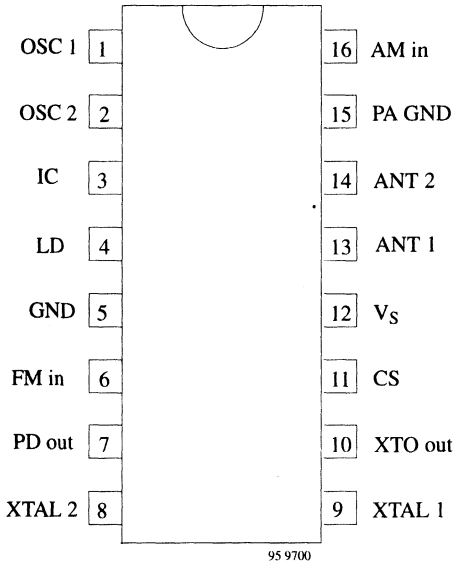
Applications

- Keyless entry (automotive, domestic,...)
- Alarm systems
- Remote control
- Communication systems

Block Diagram



Pin Description



Pin	Symbol	Function
1	OSC 1	VCO tank
2	OSC 2	VCO tank
3	IC	Internally connected
4	LD	Lock-detect (open collector)
5	GND	Ground
6	FM in	FM modulation input
7	PD out	Phase detector output
8	XTAL 2	FM modulation capacitor
9	XTAL 1	XTAL
10	XTO out	XTO output (open collector)
11	CS	Chip-select (power-up)
12	V_S	Supply voltage
13	ANT 1	Differential output 1
14	ANT 2	Differential output 2
15	PA GND	Power amplifier ground
16	AM in	AM modulation input

Absolute Maximum Ratings

All voltages are referred to GND (Pin 5). $T_A = 25°C$, unless otherwise specified.

Parameters		Symbol	Min.	Max.	Unit
Supply voltage	Pin 12	V_S	2.4	6.2	V
Output current Lock-detect	R4 = 2.7 kΩ connected to V_S = 3 V Pin 4	I4		1	mA
Output current XTO out	R10 = 2.7 kΩ connected to V_S = 3 V Pin 10	I10		1	mA
Input current AM in	R16 = 2.7 kΩ connected to V_S = 3 V Pin 16	I16		0.5	mA
Junction temperature		T_{jmax}		125	°C
Storage temperature		T_{stor}	–40	125	°C

Operating Range

All voltages are referred to GND (Pin 5). $T_A = 25°C$, unless otherwise specified.

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 12	V_S	2.4	3.0	6.2	V
Ambient temperature		T_{amb}	–40		85	°C

Maximum Thermal Resistance

All voltages are referred to GND (Pin 5). $T_A = 25°C$, unless otherwise specified.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance	R_{thJA}		120		K/W

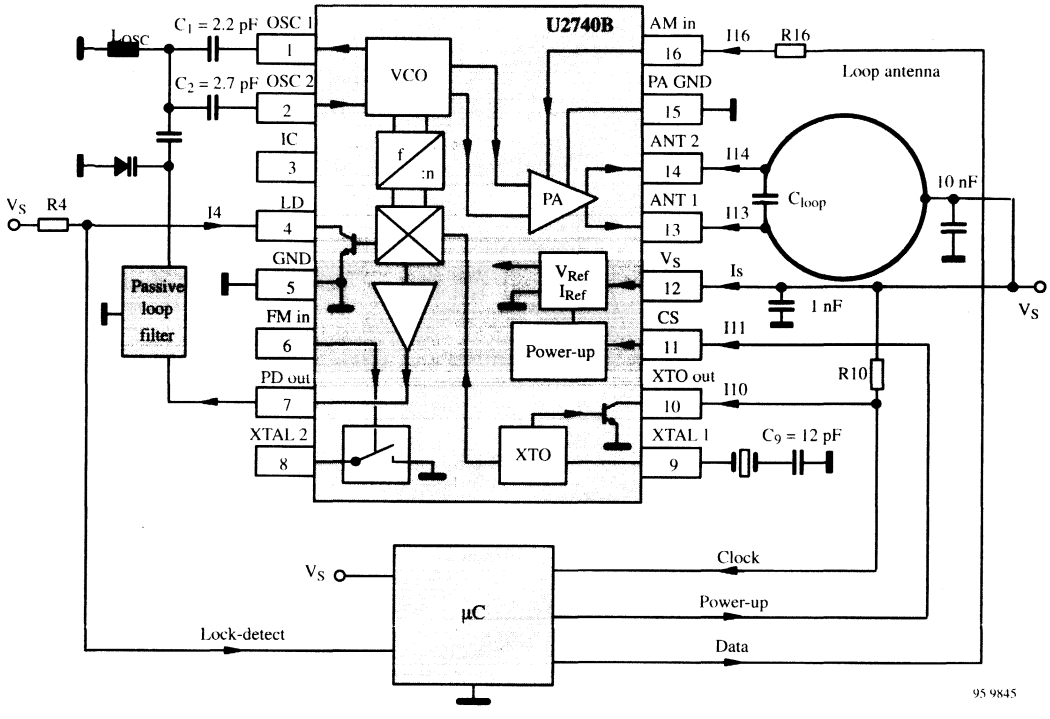
Electrical Characteristics

Test conditions (unless otherwise specified): $V_S = 3$ V, $T_{amb} = 25°C$

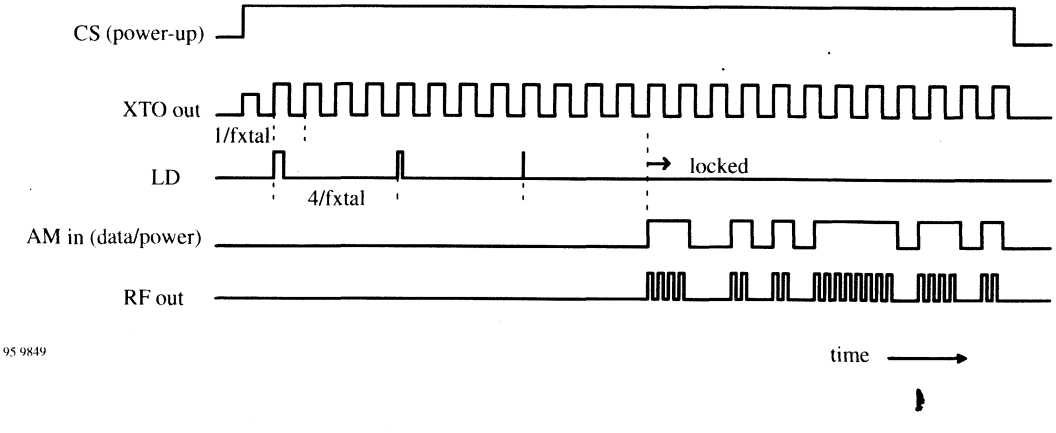
Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current (power-down)	V11 = 0, I16 = 0 Pin 12	$I_{S, OFF}$		0.05	1	µA
Supply current (power-up)	V11 = 3 V, I16 = 0 V11 = 3 V, I16 = 0.4 mA Pin 12	$I_{S, ON}$ $I_{S, ON,0.4}$		5.0 9.5		mA
Power-down voltage	I16 = 0 Pin 11	$V_{11,OFF}$			0.4	V
Power-down current	V11 = 0, I16 = 0 Pin 11	$I_{11, OFF}$			0.1	µA
Power-up voltage	I16 = 0 Pin 11	$V_{11,ON}$	1.0			V
Power-up current	V11 = 3 V, I16 = 0 Pin 11	$I_{11, ON}$		40		µA
Output power (f_{VCO} = 433.92 MHz)	V11 = 3 V I16 = 0 V11 = 3 V I16 = 0.4 mA Pins 13 and 14	$P_{out, OFF}$ $P_{out, ON}$		–40 0		dBm dBm
Hold in range	Pins 13 and 14	Δf_H				MHz
Phase detector Output current	Pin 7	I_{PD}	–1		1	mA
Enable settling time	Pins 11/13 and 14	T_{enable}				µs
Output frequency range	Pins 13 and 14	f_{VCO}	200		500	MHz
XTO frequency range	Pins 9 and 10	f_{XTO}	3		6	MHz
Input current AM in	R16 = 0 connected to V_S Pin 16	I16		0.5		mA
Amplitude modulation bandwidth	Pin 16	BW_{AM}				kHz
Input current FM in	V6 = 3 V Pin 6	I6		16		µA
Frequency modulation bandwidth	Pin 6	BW_{FM}				kHz
Output current Lock-detect	R4 = 27 kΩ connected to V_S Pin 4	I4 [1]		0.1		mA
Output current XTO out	R10 = 27 kΩ connected to V_S Pin 10	I10 [1]		0.1		mA

Note: [1] depends on value of resistor connected to V_S

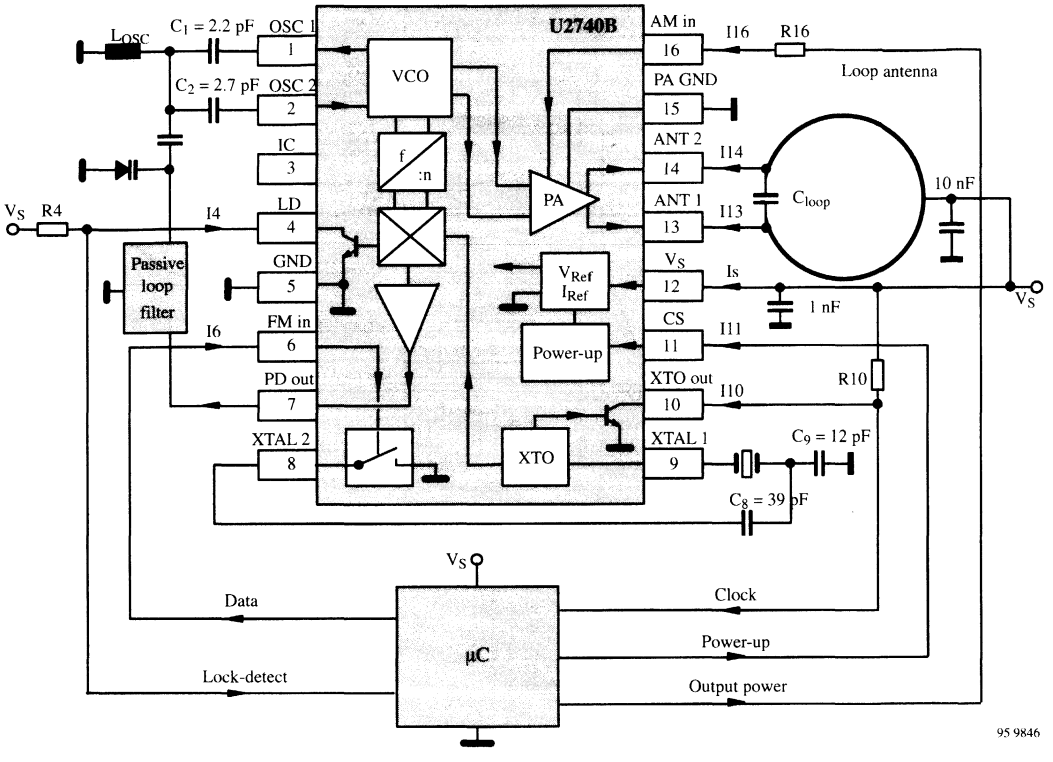
Application Circuit (AM Modulation)



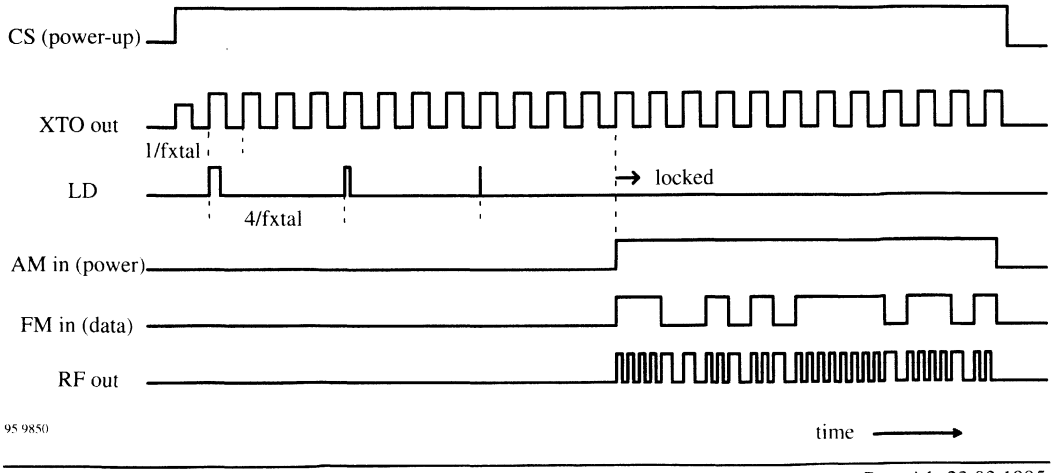
Principle of Operation (AM Modulation)



Application Circuit (FM Modulation)

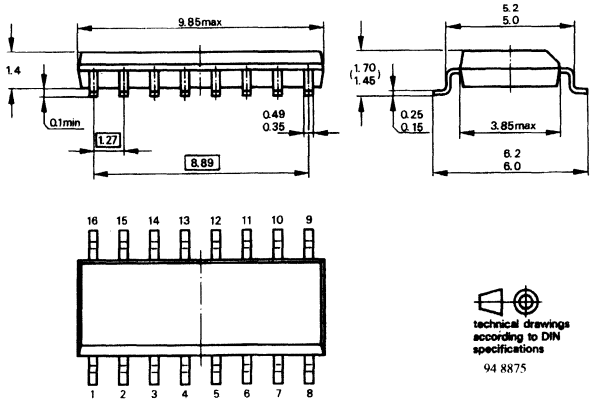


Principle of Operation (FM Modulation)



Dimensions in mm

Package: SO 16



Infrared Driver

Description

The U426B is an IR-driver-IC for IR data communication. The circuit contains a programmable constant current source (DRV) to drive the IRED. The current is programmed by an external resistor (RS). With the internal comparator (COMP) an external voltage can be monitored. The low power standby mode, controlled by means of the WAKE input, makes the circuit well suited for battery powered systems.

Features

- Programmable constant current 200 mA to 1.2 A
- Signal frequency up to 500 kHz
- Low power standby mode
- Internal voltage comparator
- Wide voltage range 2.4 to 12 V

Applications

- Keyless entry systems
- Remote control
- Wireless data communication

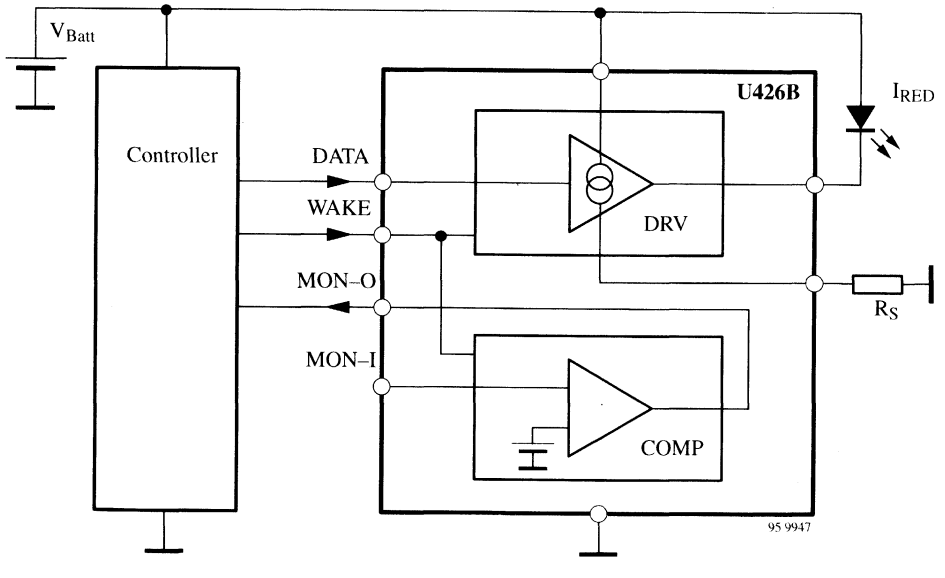
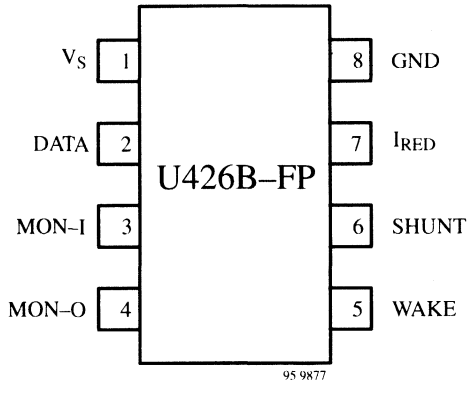


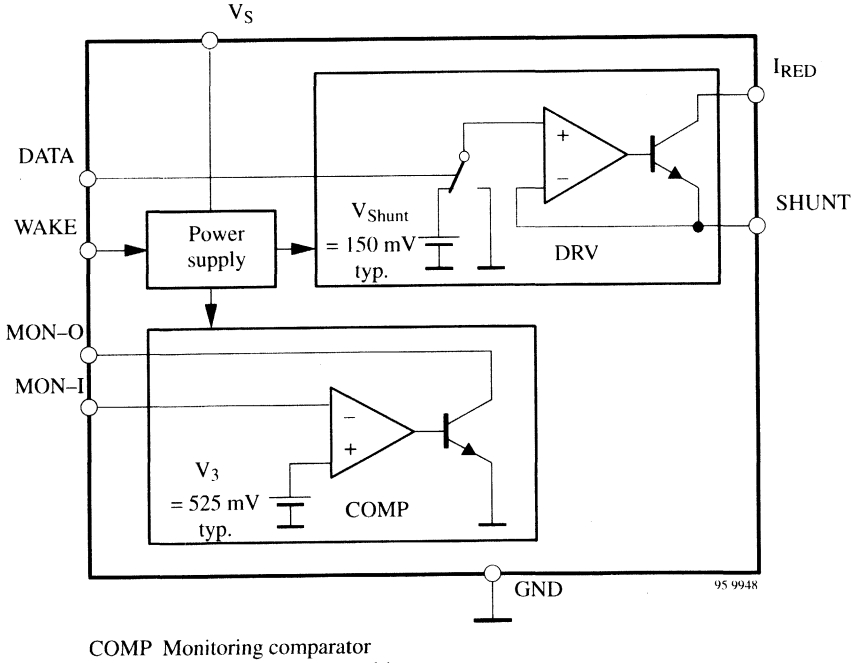
Figure 1.

Pin Description



Pin	Symbol	Function
1	V_S	Supply voltage
8	GND	Circuit ground
2	DATA	Data input for switching the IRED output current on and off
7	IRED	IR-LED output, when the data input is high this output supplies the IR-LED with the constant current
6	SHUNT	The resistor at this pin adjusts the IRED output current
3	MON-I	Voltage monitor input of the internal comparator
4	MON-O	Voltage monitor output. This open collector output is active when the voltage at MON-I is below the internal reference V_3 = 525 mV typ.
5	WAKE	WAKE input. When LOW the circuit is in standby mode. A high level activates the circuit

Block Diagram



COMP Monitoring comparator
DRV IRED constant current driver

Figure 2.

Constant Current Driver (DRV)

The constant current driver converts the incoming data pulses into adequate constant current pulses. A high level applied to the data-input causes a constant current flow through the IR-diode connected to the IRED output. This current can be programmed via the external resistor (RS). To calculate the output current, use the following formula:

$$I_{RED} = 150\frac{mV}{R_S}$$

Power Supply

The power supply circuit generates the internal supply voltage from an external voltage (V_S = 2.4 to 12 V).The V_S-pin is protected by an internal suppressor diode against voltages above 13 V. The internal supply voltage can be switched on/off with a high/low-level at the WAKE input. Setting WAKE to low level switches the circuit from busy to standby mode, which results in a very low, current consumption (2 µA). Every change between busy and standby mode needs a latency up to 1 ms. Data transmission and voltage monitoring only takes place while WAKE remains high.

Monitoring Comparator (COMP)

The monitoring comparator compares the voltage at pin MON-I to an internal reference voltage of V_3 = 525 mV typ. The open collector output transistor is active, if the voltage at pin MON-I falls below the internal threshold voltage. The comparator can be used to monitor the power supply battery.

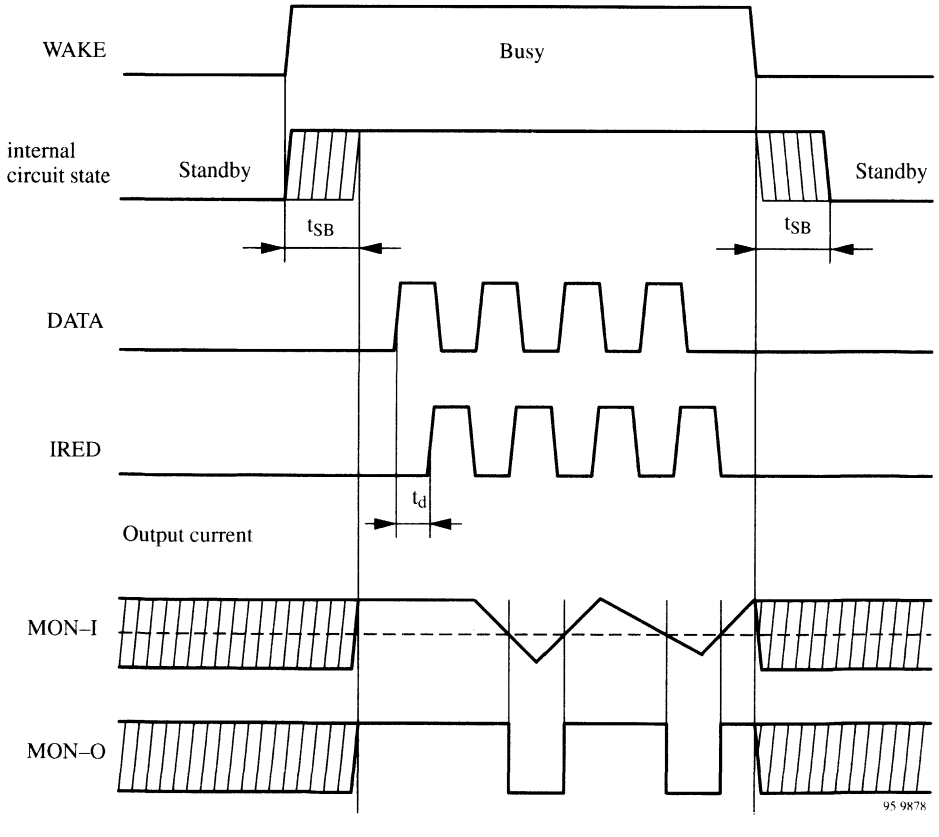


Figure 3. Timing diagram

Absolute Maximum Ratings

Parameters		Symbol	Value	Unit
Supply voltage	Pin 1	V_S	13.4	V
Supply current		I_S	40	mA
$t < 10\ \mu s$		i_s	150	mA
Input voltages	Pin 2, 3 and 5	V_I	V_S	V
	Pin 6		1	V
Input currents	Pins 2, 3 and 5	I_I	1	mA
Output voltage	Pin 7	V_7	13.4	V
	Pin 4	V_4	V_S	V
Output current		I_7	1.5	A
$t < 100\ \mu s$	Pin 7	I_4	5	mA
	Pin 4			
Power dissipation				
$T_{amb} = 85°C$				
SO 8 : on p.c. board		P_{tot}	150	mW
on ceramic		P_{tot}	250	mW
on ceramic with silicon grease		P_{tot}	430	mW
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	–40 to 85	°C
Storage temperature range		T_{stg}	–40 to 150	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient			
SO 8: on p.c. board	R_{thJA}	220	K/W
on ceramic	R_{thJA}	140	K/W
on ceramic with silicon grease	R_{thJA}	80	K/W

Electrical Characteristics

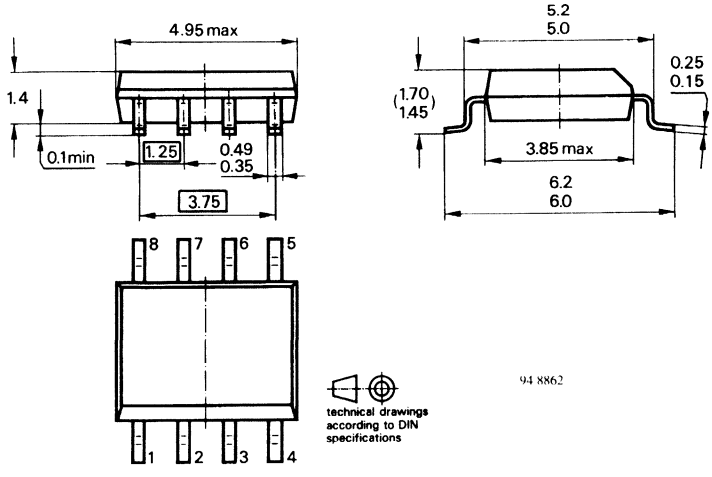
$V_S = 6$ V, $T_{amb} = 25°C$, reference point pin 8, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current	**Pin 1**					
Supply voltage	Pin 1	V_S	2.4		12	V
Standby current		I_I			2	µA
Wake-up current	Without pulse	I_I			1.5	mA
Overvoltage protection	$I_I = 20$ mA	V_S		13		V
DATA	**Pin 2**					
Input signal	High	V_2	3	3.6	4.2	V
	Low	V_2	1.6	2.1	2.6	V
Common mode input			0		V_S	V
Rise time		t_r			500	ns
Fall time		t_f			500	ns
Signal frequency		f			500	kHz
Input current		I_2			100	µA

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
MON-I	**Pin 3**					
Input current	V_3 = 6 V	I_3			0.3	µA
Reverse current	V_3 = 0 V	I_r			0.8	µA
Input voltage high	MON-I on	V_3	485	525	555	mV
Input voltage low	MON-O off	V_3	515	545	580	mV
Hysteresis				4		%
Temperature coefficient		TC		100		µA/K
MON-O	**Pin 4**					
Output current	$V_4 \geq 200$ mV	I_4	1			mA
Output current	$V_4 \geq 400$ mV	I_4	3			mA
Reverse current	$V_4 \leq 6$ V	I_r			0.2	µA
Output voltage High					V_S	V
Saturation voltage	I_4 = 1 mA	V_{sat}			200	mV
WAKE	**Pin 5**					
Input current	V_5 = 6 V	I_5			80	µA
	V_5 = 0 V	I_5			±0.2	µA
Input voltage High	Busy	V_5			V_S	V
Input voltage LOW	Standby	V_5	0		0.2	V
SHUNT	**Pin 6**					
Output current IRED	V_S = 2.4 V; R_S = 0.62 Ω	I_7	205		245	mA
	V_S = 6.0 V; R_S = 0.62 Ω	I_7	220		265	mA
	V_S = 12 V; R_S = 0.62 Ω	I_7	235		275	mA
	V_S = 6 V; R_S = 0.11 Ω	I_7	1.25		1.5	A
	V_S = 12 V; R_S = 0.11 Ω	I_7	1.3		1.55	A
Shunt voltage	$V_2 = V_S$ = 6 V; R_S = 0.11 Ω	V_{Shunt}	140	150	160	mV
Temperature coefficient	T_{amb} = –40 to 85°C	T_C		40		µV/K
IRED	**Pin 7**					
Output voltage	$V_2 = V_S$ = 6 V; I_7 = 1 A	V_{out}			1000	mV
Output voltage	V_2 =0 V; I_7 = 0	V_{out}		12	13.2	V
Reverse current	V_2 =0 V; V_7 = 6 V	I_r			1	µA
Rise/Fall time		t_r			300	ns
Delay time	Pin 2 to pin 7	t_d			1	µs
Standby/Busy		t_{SB}			1	ms
Busy/Standby		t_{BS}			1	ms

Dimensions in mm

Package: SO 8



Low–Current Superhet Remote Control Receiver

Description

The U4311B is a monolithic Integrated Circuit in bipolar technology for low-current UHF remote control superheterodyne receivers in amplitude- or frequency-modulated mode. Typical applications are keyless car lock-, alarm or telecontrol remote indication systems. Especially for automotive applications it supports a superhet design with about 1 mA total current consumption, as required by the car manufacturers.

Features

- Usable for amplitude- and frequency- modulated transmission systems
- Extremely low quiescent current approximately 1 mA in the stand-by mode due to wake-up concept
- Wide power supply voltage range 3 to 13 V
- Sensitive IF-amplifier for 10.7 MHz operating frequency
- Logarithmic AM demodulator
- FM demodulator
- Monoflop exit to wake up a microcontroller
- High performance operational amplifier to realize a data recovering filter
- Non-inverting clamping comparator with amplitude-depending hysteresis for data regeneration

Block Diagram

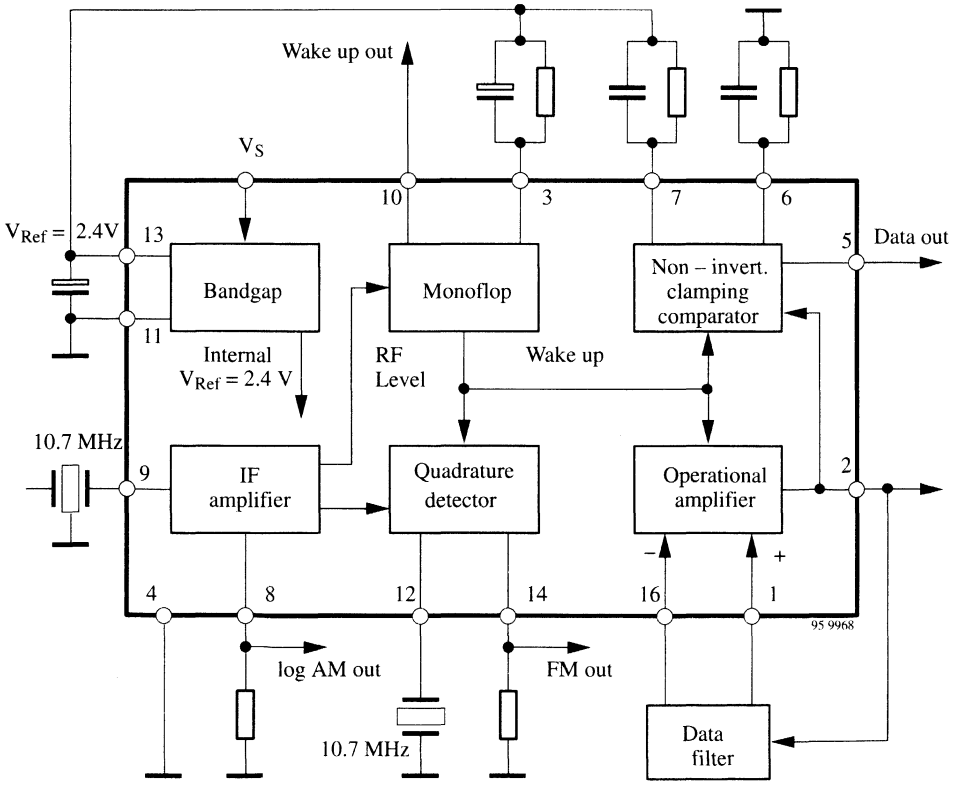


Figure 1. Block diagram

Pin Description

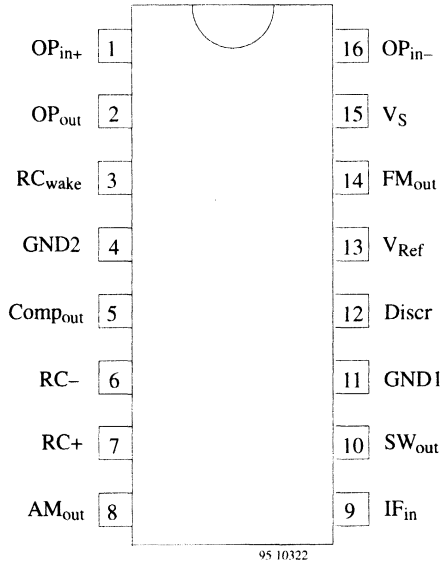


Figure 2. Pin description

Pin	Symbol	Function
1	OP_{in+}	OP amplifier non inverted input
2	OP_{out}	OP amplifier output
3	RC_{wake}	RC wake up reset time
4	GND2	Ground of the logical circuits
5	$Comp_{out}$	Comparator output
6	RC–	Comparator time constant
7	RC+	Comparator time constant
8	AM_{out}	AM current output
9	IF_{in}	IF input
10	SW_{out}	Wake up output
11	GND1	Ground of the analog circuits
12	Discr	FM discriminator tank
13	V_{ref}	Reference voltage
14	FM_{out}	FM discriminator output
15	V_S	Supply voltage
16	OP_{in-}	OP amplifier inverted input

Internal connections see figures 4 to 19

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_S	13	V
Power dissipation $T_{amb} = 85°C$	P_{tot}	400	mW
Junction temperature	T_j	125	°C
Ambient temperature	T_{amb}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Thermal Resistance

Parameters		Symbol	Value	Unit
Junction ambient	DIP16	R_{thJA}	120	K/W
	SO16L	R_{thJA}	100	K/W

Electrical Characteristics

V_S = 5 V, T_{amb} = 25°C, f_{in} = 10.7 MHz: FM part: f_{mod} = 1 kHz, f_{dev} = 22.5 kHz; AM part: f_{mod} = 1 kHz, m = 100% unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Characteristics						
Supply voltage range	Pin 15	V_S	3		12	V
Quiescent supply current	Pin 15	I_q		1	1.3	mA
Active supply current	Pin 15	I_{act}		2.8	3.6	mA
Bandgap						
Regulated voltage	Pin 13	V_{ref}	2.3	2.4	2.5	V
Output current	Pin 13	I_{ref}			5	mA
Source resistance	Pin 13	R_{ref}		2.3	5	Ω
External capacitor	Pin 13	C_{ref}	10			µF
Power supply rejection ratio	f = 50 Hz Pin 13	psrr		60		dB
IF amplifier						
Input resistance	Pin 9	R_{in}	180	330	520	Ω
Input capacitance	Pin 9	C_{in}		5		pF
Typical internal 3 dB frequency	IF level 70 dBµV Pins 9 and 14	f_{3dB}	8		12	MHz
–3 dB limiting point	Pin 9	V_{FM3dB}		30		dBµV
Recovered data voltage	Pin 14	V_{FMout}	50	130	230	mV
FM detector output resistance	Pin 14	R_{FMout}		50		kΩ
AM rejection ratio	m = 30% Pins 9 and 14	AM_{rr}		25		dB
Maximum AM input voltage	Pin 9	V_{AMmax}		90		dBµV
AM quiescent current	Pin 8	I_{AMout}	10	22	37	µA
Maximum AM current	Pin 8	$I_{AMoutmax}$		100		µA
Operational amplifier						
Gain bandwidth product	Pins 1, 2 and 16	f_t	3	4	6.5	MHz
Excess phase	Pins 1, 2 and 16	δ		80		degree
Open loop gain	Pins 1, 2 and 16	g_0	50	70	95	dB
Output voltage range	Pin 2	ΔV_{out}		1.55		V
Common mode input voltage	Pins 1 and 16	V_{in}	0.7		1.7	V
Input offset voltage	Pins 1 and 16	V_{os}	–2.5	0	+2.5	mV
Maximum output current	Pin 2	I_{out}			5	mA
Common mode rejection ratio	Pin 1 and 16	cmrr	65	85		dB
Total harmonic distortion	V_{in} < 300 mV, f = 33 kHz, unity gain circuit Pin 2	thd		1	3	%
Power supply rejection ratio	f = 50 Hz Pin 2	psrr	65	85		dB

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Clamping comparator						
Typical common mode input voltage range	Pin 2	V_{cmvr}	0.8		1.6	V
Maximum distortion voltage	V_{signal} = 100 mV, R+ = R– = 50 kΩ, C+ = C– = 200 nF, f_{disto} = 50 Hz, f_{signal} = 1 kHz Pin 2	V_{dmax}			200	mV
Output voltage	$V_2 > (V_6 + V_7)/2$ (10 kΩ load to V_{Ref}) Pin 5	V_{cout}		V_{Ref}		1)
Output voltage	$V_2 < (V_6 + V_7)/2$ (10 kΩ load to V_{Ref}) Pin 5	V_{cout}	0	150	250	mV
Wake up circuit						
Minimum wake up level	Pin 9	V_{in}		40		dBµV 2)
Internal charging resistor	Pin 3	R_{int}		1.5		kΩ
Threshold voltage	Pin 3	V_{th}		1.6		V
Output switch current	Pin 10	I_{SW}	180	250	550	µA
Output switch voltage	Pin 10	V_{SW}			5.5	V 3)
External wake up resistor	Pins 3 and 13	R_{WU}	22			kΩ
External wake up capacitor	Pins 3 and 13	C_{WU}			10	µF
Hold time (± 30%)		t_h	$\approx 1.5 \times R_{WU} \times C_{WU}$			s 4)
Delay time (± 30%)		t_d	$\approx C_{WU} \times 0.75$ kΩ			s 4)

1) IC version with inverting comparator available: U4313B

2) Measured at Pin 9, referred to 330 Ω

3) Protected by a Z-diode, see figure 13

4) Valid for 0.1 µF ≤ C_{WU} ≤ 10 µF and 22 kΩ ≤ R_{WU} ≤ 680 kΩ

Application

The U4311B is well-suited to implement UHF remote control or data transmission systems, based on a low-current superheterodyne receiver concept. SAW-devices may be used in the transmitter as well as in the receiver local oscillator. The front end should be a discrete circuit application with low current UHF-transistors like S822T or S852T from TEMIC TELEFUNKEN microelectronic GmbH. The frequency of the local oscillator can be determined either by coaxial resonators or SAW-devices. Due to large SAW-resonator tolerance an IF-bandwidth – and in a FM-system additionally the discriminator amplitude characteristic (figure 28) – of 300 kHz or higher is proposed. As the circuit needs only 3.0 V supply voltage for operation the front end may be a stacked design in order to achieve a total receiver current consumption of approximately 1 mA. Figure 29 shows a principle receiver concept diagram. The application notes ANT012, ANT013, and ANT015 contain more detailed information on complete RF links.

Circuit Description

General functions

The integrated circuit U4311B includes the following functions: IF-amplifier, FM-demodulator, wake-up circuit with monoflop, operational-amplifier, non-inverting data comparator and voltage-regulator.

The 10.7 MHz IF-signal from the front end passes the integrated IF-amplifier which operates for amplitude- or frequency-modulated signals to either a logarithmic AM-demodulator which was implemented to avoid settling time problems effected by use of an automatic gain control system or a quadrature detector for FM. A data shaping filter – advantageously realized with the internal high performance operational-amplifier – reduces system bandwidth to an optimized compromise regarding transmission distance and data recognition. Thus, an optimal bit error rate can be achieved without any further active component.

The comparator connected to the output of the filter has a level-dependent hysteresis and clamps its reference voltage to the signal minimum and maximum peaks as described later.

Without IF-input signal – in the normal mode – only the IF-amplifier and the AM demodulator which operates as a level strength indicator are activated. If the level of the IF signal increases, the whole circuitry is turned on by the wake-up circuit. This signal is externally available at pin 10 and can be used to wake up a microcontroller. After an adjustable reset time, determined by the mono-flop time constant, the integrated circuit rests down to the sleep mode. In this case typically 1 mA supply current is required. An external resistor matched at pin 3 to ground blocks the wake-up circuit and gives fully function at lower IF-level as to recognize in figures 24 and 27, but supply current increases up to typically 2.8 mA.

Function of the clamping comparator

The output signal of the operational amplifier is fed to the input of the non-inverting comparator and two peak detectors (Q1 and Q2, figure 3). Their time constants are distinguished by RC+ and RC–. The components value must be adapted to the transmission code. The time constant should be large compared to the bit-rate for optimized noise and hum suppression. To compensate the input transistors base-emitter-voltage differences these two signals are buffered by Q3 and Q4. The mean value is used as comparator threshold, the difference of the peak values controls the hysteresis. This clamping comparator works as a data regenerator.

Another version of the IC, with an inverting clamping comparator, is also available (U4313B). Therefore the operational amplifier can be used either as a non-inverting or an inverting filter without the need of any additional components.

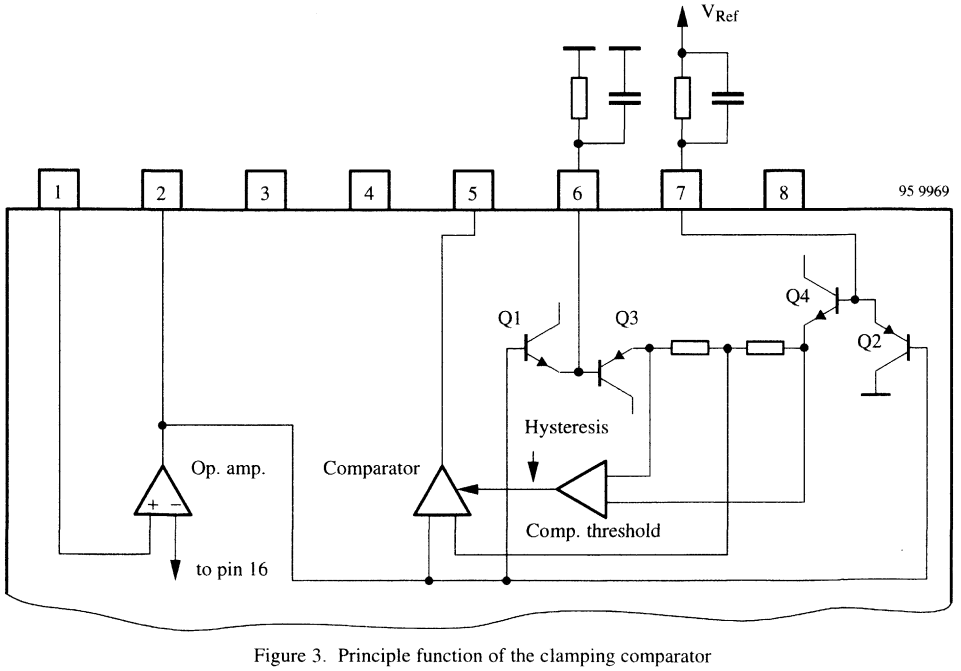


Figure 3. Principle function of the clamping comparator

Internal Pin Circuitry

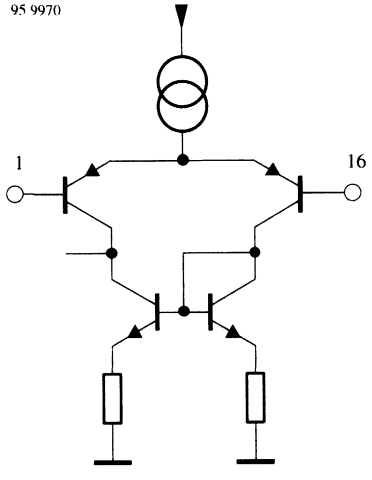


Figure 4. Pin 1 OP_{in+}

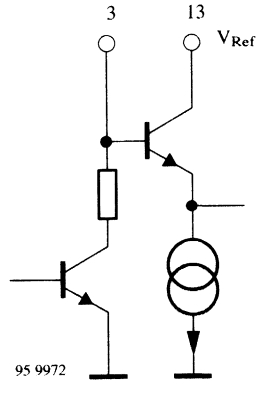


Figure 6. Pin 3 RC_{wake}

Figure 7. Pin 4 GND2

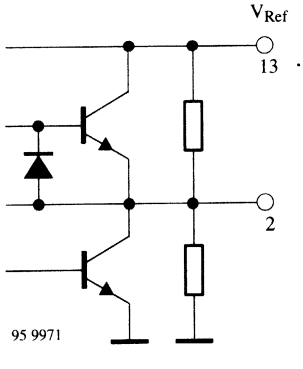


Figure 5. Pin 2 OP_{out}

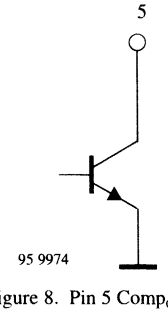


Figure 8. Pin 5 $Comp_{out}$

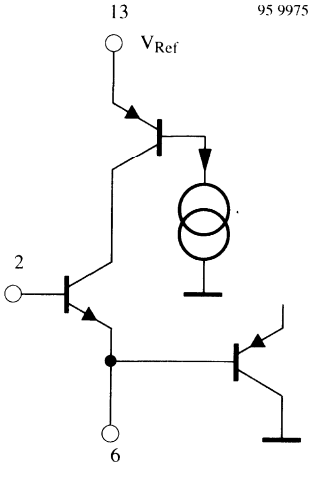


Figure 9. Pin 6 RC–

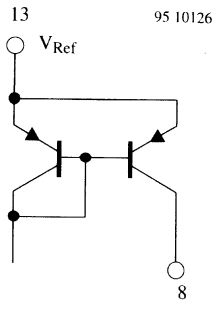


Figure 11. Pin 8 AM_{out}

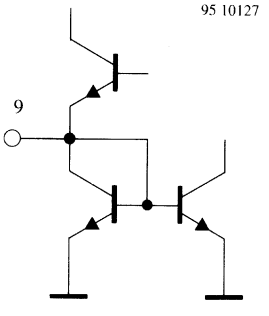


Figure 12. Pin 9 IF_{in}

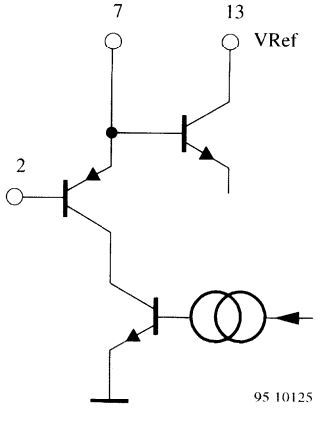


Figure 10. Pin 7 RC+

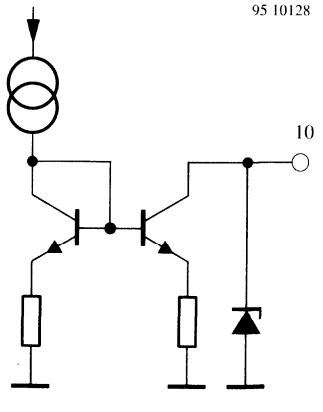


Figure 13. Pin 10 SW_{out}

Figure 14. Pin 11 GND1

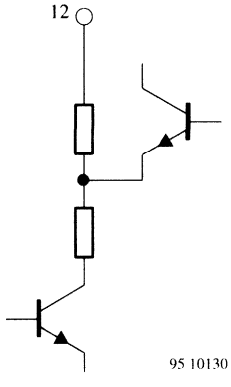


Figure 15. Pin 12 Discr

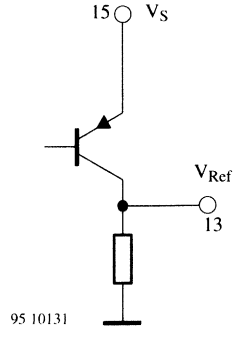


Figure 16. Pin 13 V_{Ref}

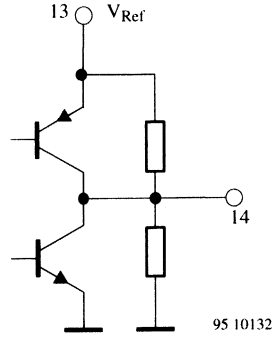


Figure 17. Pin 14 FM_{out}

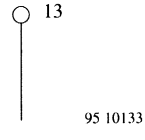


Figure 18. Pin 15 V_S

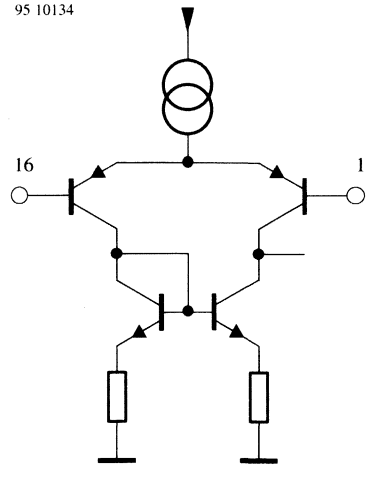


Figure 19. Pin 16 OP_{in-}

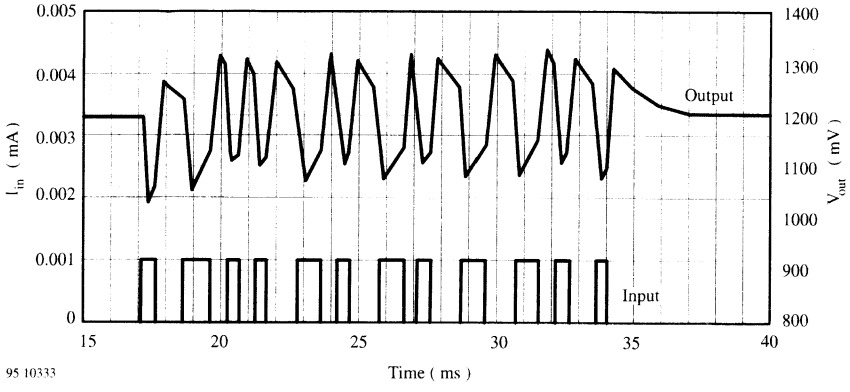


Figure 20. Time domain response of 2 kHz Bessel low pass data filter

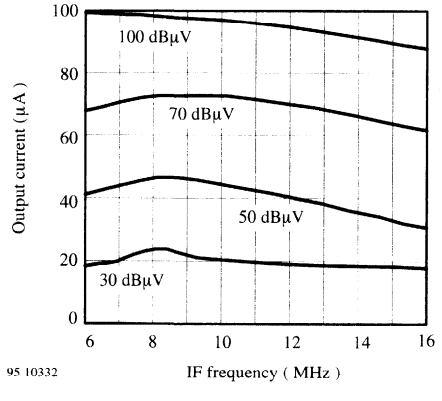


Figure 21. IF-frequency response

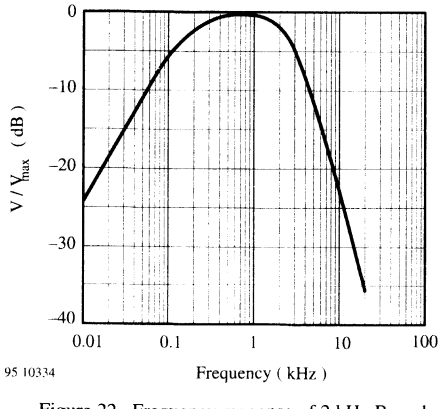


Figure 22. Frequency response of 2 kHz Bessel low pass data filter

Data Recovering Filter

The test circuit in figures 23 and 26 includes an example of a data recovering filter realized with the components R_1, R_2, C_1, C_2, C_3. It is of a second order Bessel type with low pass characteristic, a 3 dB cut-off frequency of 2 kHz and an additional high pass characteristic for suppressing dc and low frequency ac components. Simulation of time domain and frequency response is drawn in figures 20 and 22. This filter gives a typical application of a 1 kBaud Manchester code amplitude modulated transmission.

The capacitor C_2 is responsible for the high pass cut-off frequency. For a correct pulse response this high pass cut-off frequency should be as low as possible. Figure 20 shows the transient response and the influence of the dc component. The first pulses might be wrong if the high pass cut-off frequency is too low. For this reason some burst bits must be transmitted before the real data transmission starts. On the other hand, if the cut-off frequency is too high, you might get in trouble with roof shaping of the rectangle pulses at the operational amplifier output.

The low pass cut-off frequency and the maximum transimpedance V_{out}/I_{in} are distinguished by the further external elements. Careful design of the data filter gives optimized transmission range. For designing other filter parameters look for filter design handbooks or programs or request TEMIC TELEFUNKEN microelectronic GmbH for support. Some proposals can be found in the application notes ANT012, ANT013 and ANT015.

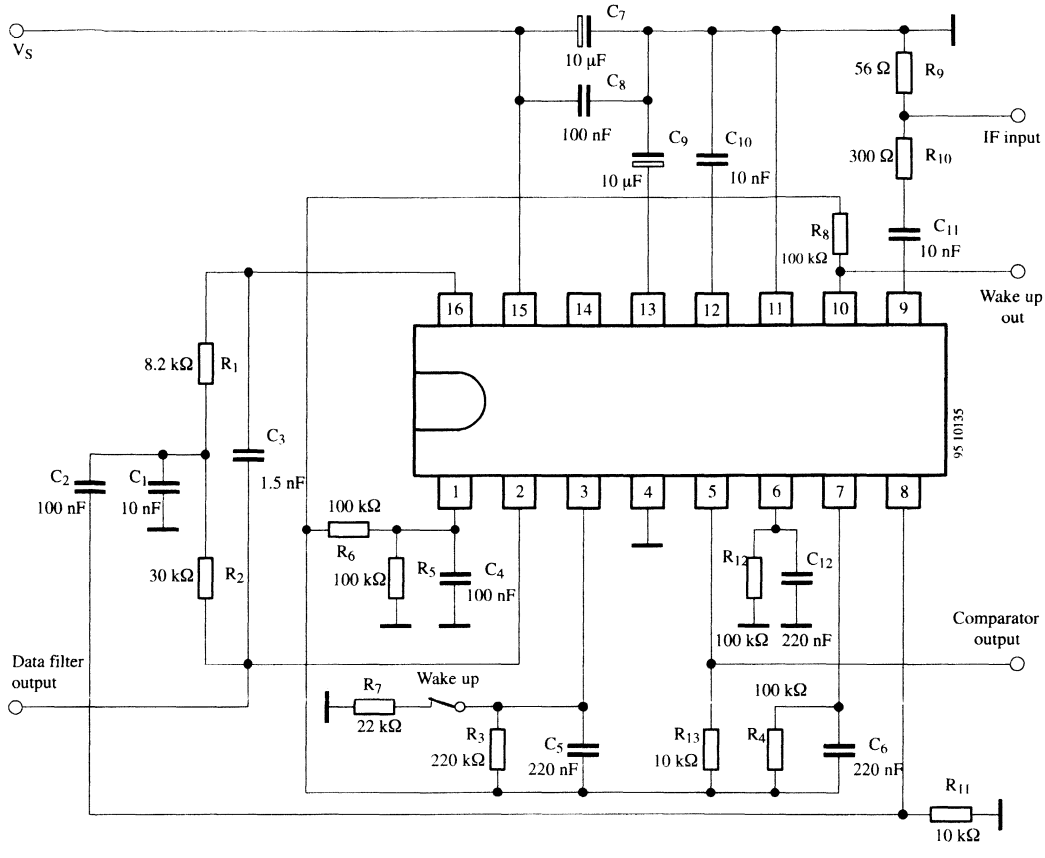


Figure 23. AM test circuit with 2 kHz Bessel low pass data filter

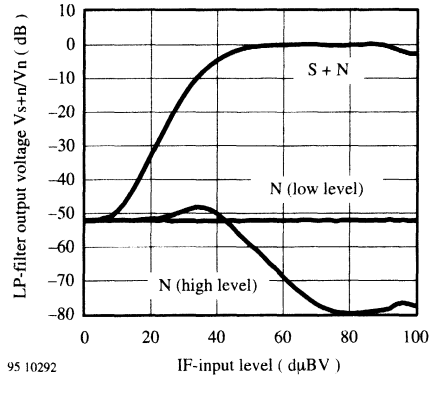


Figure 24. Signal to noise ratio AM

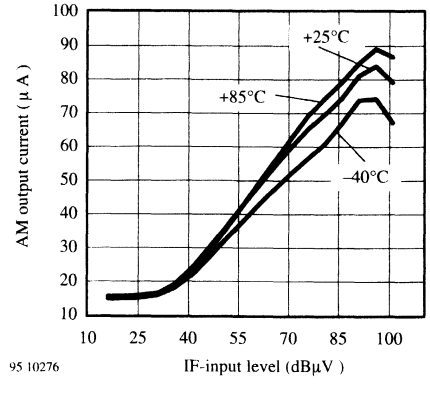


Figure 25. AM-demodulator characteristic vs. temperature

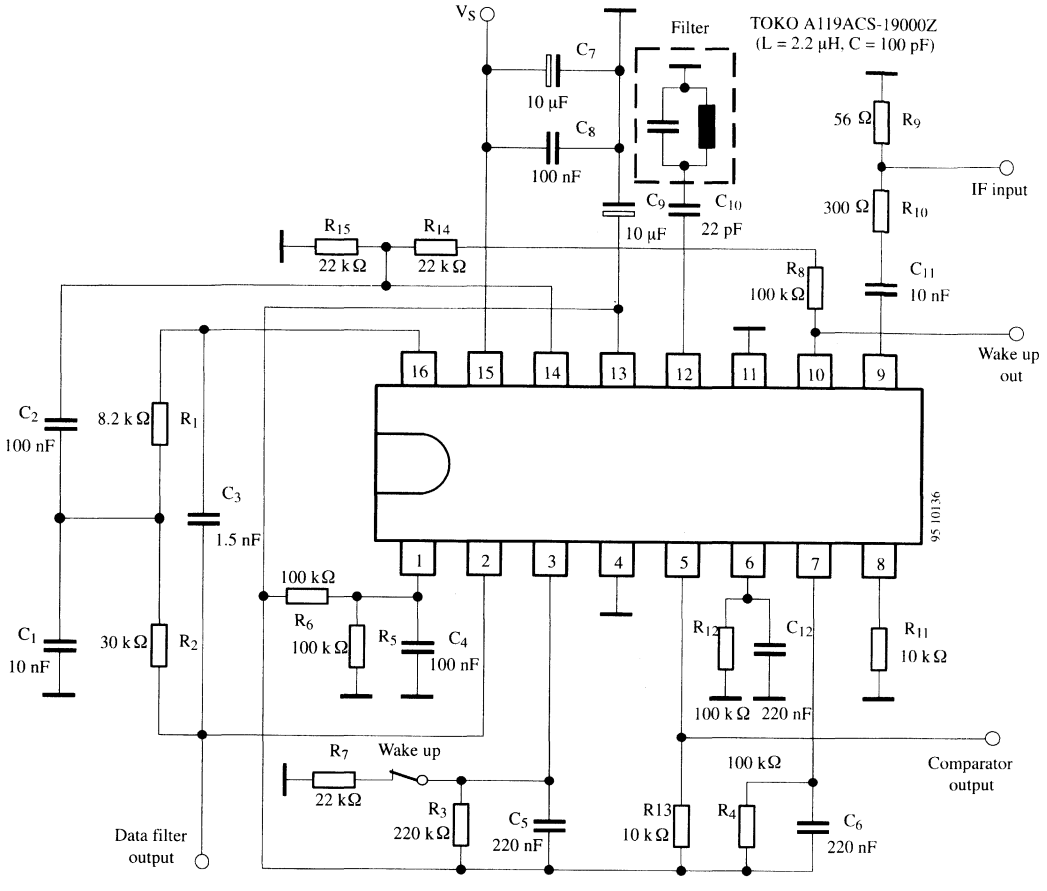


Figure 26. FM test circuit with 2 kHz Bessel low pass data filter

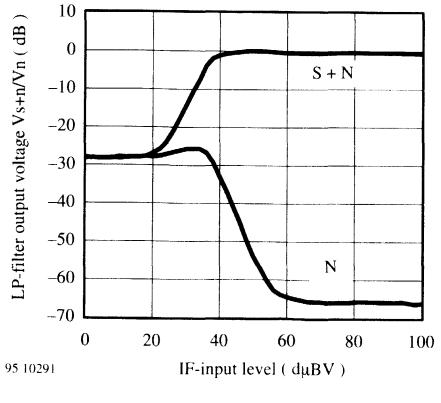


Figure 27. Signal to noise ratio FM; deviation 22.5 kHz

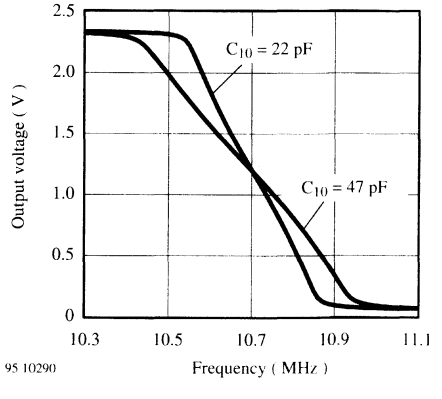


Figure 28. FM-discriminator characteristic

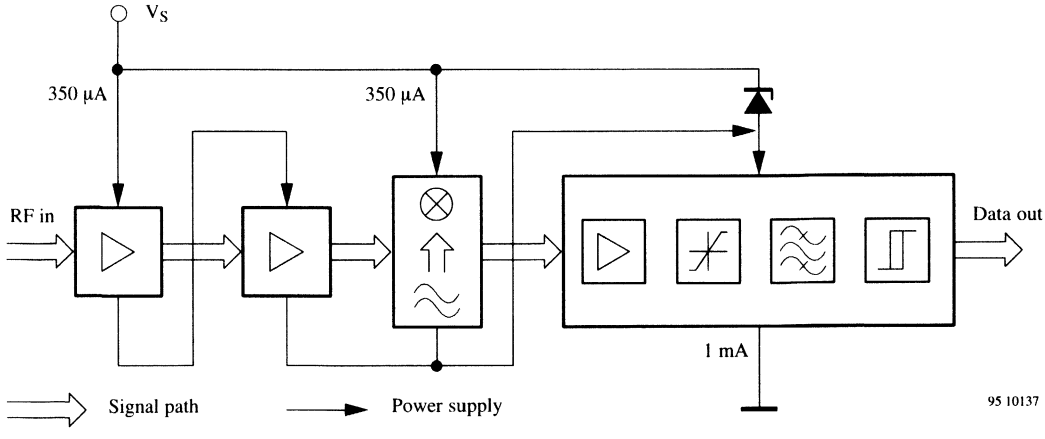


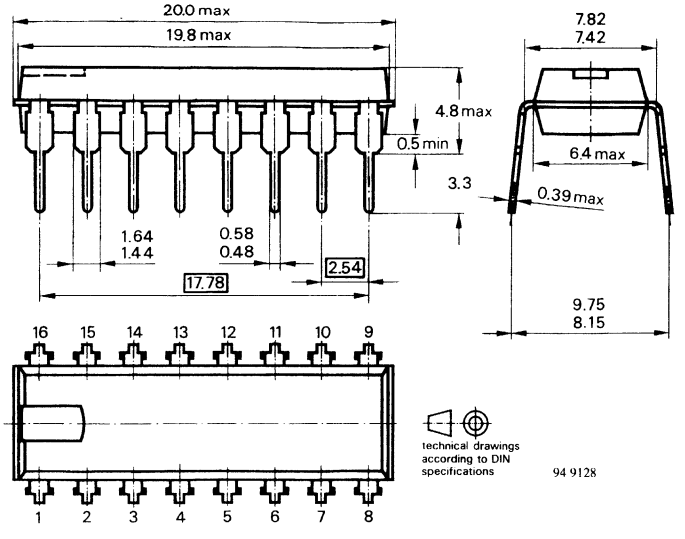
Figure 29. Principle diagram UHF remote control receiver

Ordering Information

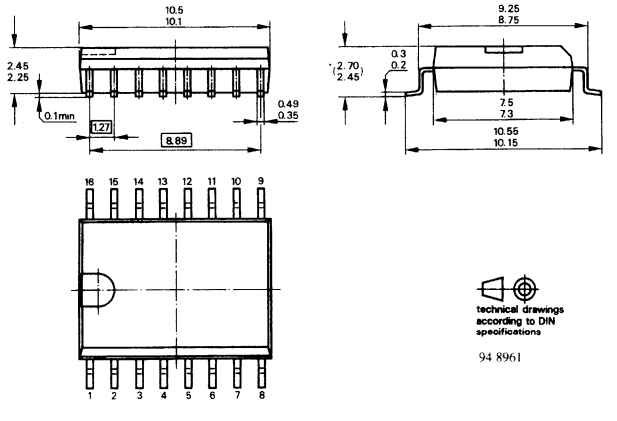
Extended Type Number	Package	Remarks
U4311B-C	DIP16	
U4311B-CFL	SO16L	

Dimensions in mm

Package: DIP16



Package: SO16L



Low-Current Superhet Remote Control Receiver

Description

The U4313B is a monolithic integrated circuit in bipolar technology for low-current UHF remote control superheterodyne receivers in amplitude- or frequency-modulated mode. Typical applications are keyless car lock-, alarm or telecontrol remote indication systems. Especially for automotive applications it supports a superhet design with less than 1 mA total current consumption, as required by the car manufacturers.

Features

- Usable for amplitude- and frequency-modulated transmission systems
- Extremely low quiescent current approximately 1 mA in the stand-by mode due to wake-up concept
- Wide power supply voltage range 3 to 13 V
- Sensitive IF-amplifier for 10.7 MHz operating frequency
- Logarithmic AM demodulator
- FM demodulator
- Monoflop exit to wake up a microcontroller
- High performance operational amplifier to realize a data recovering filter
- Inverting clamping comparator with amplitude-depending hysteresis for data regeneration

Block Diagram

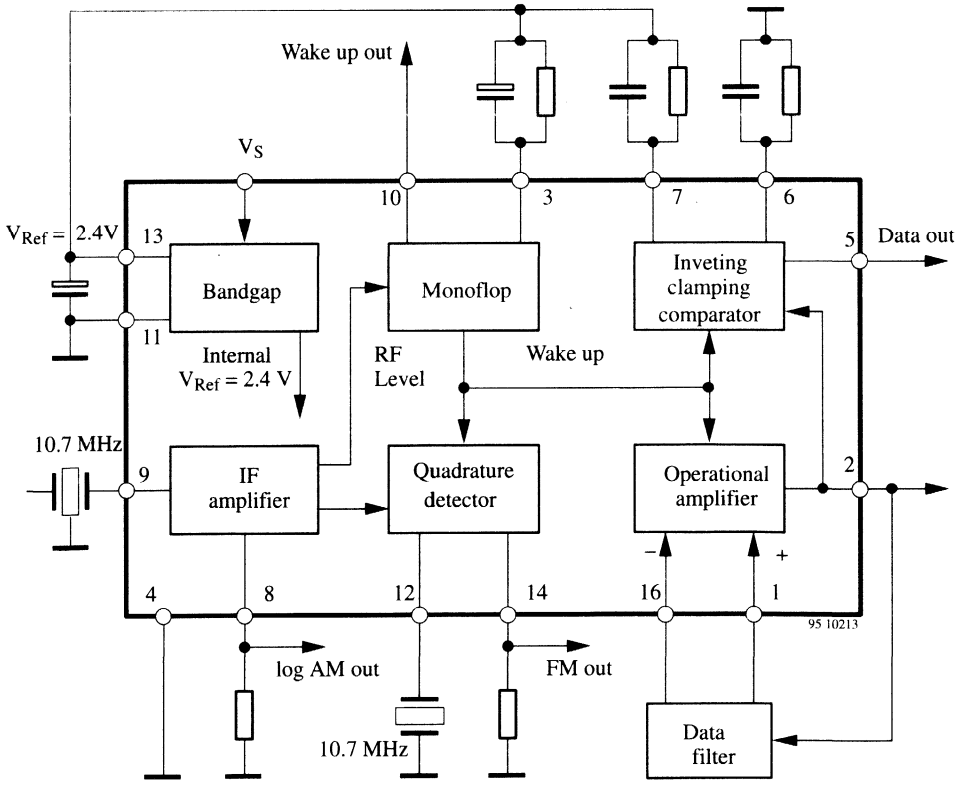


Figure 1. Block diagram

Pin Description

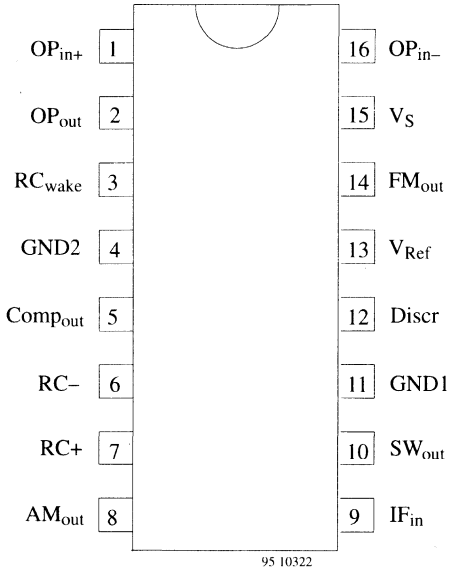


Figure 2. Pin description

Pin	Symbol	Function
1	OP_{in+}	OP amplifier non inverted input
2	OP_{out}	OP amplifier output
3	RC_{wake}	RC wake up reset time
4	GND2	Ground of the logical circuits
5	$Comp_{out}$	Inverting comparator output
6	RC–	Comparator time constant
7	RC+	Comparator time constant
8	AM_{out}	AM current output
9	IF_{in}	IF input
10	SW_{out}	Wake up output
11	GND1	Ground of the analog circuits
12	Discr	FM discriminator tank
13	V_{Ref}	Reference voltage
14	FM_{out}	FM discriminator output
15	V_S	Supply voltage
16	OP_{in-}	OP amplifier inverted input

Internal connections see figures 4 to 19

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_S	13	V
Power dissipation $T_{amb} = 85°C$	P_{tot}	400	mW
Junction temperature	T_j	125	°C
Ambient temperature	T_{amb}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Thermal Resistance

Parameters		Symbol	Value	Unit
Junction ambient	DIP16	R_{thJA}	120	K/W
	SO16L	R_{thJA}	100	K/W

Electrical Characteristics

V_S = 5 V, T_{amb} = 25°C, f_{in} = 10.7 MHz; FM part: f_{mod} = 1 kHz, f_{dev} = 22.5 kHz; AM part:, f_{mod} = 1 kHz, m = 100% unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Characteristics						
Supply voltage range	Pin 15	V_S	3		12	V
Quiescent supply current	Pin 15	I_q		1	1.3	mA
Active supply current	Pin 15	I_{act}		2.8	3.6	mA
Bandgap						
Regulated voltage	Pin 13	V_{ref}	2.3	2.4	2.5	V
Output current	Pin 13	I_{ref}			5	mA
Source resistance	Pin 13	R_{Ref}		2.3	5	Ω
External capacitor	Pin 13	C_{ref}	10			µF
Power supply suppression	f = 50 Hz Pin 13	psrr		60		dB
IF amplifier						
Input resistance	Pin 9	R_{in}	180	330	520	Ω
Input capacitance	Pin 9	C_{in}		5		pF
Typical internal 3 dB frequency	IF level 70 dBµV Pins 9 and 14	f_{3dB}	8		12	MHz
–3 dB limiting point	Pin 9	V_{FM3dB}		30		dBµV
Recovered data voltage	Pin 14	V_{FMout}	50	130	230	mV
FM detector output resistance	Pin 14	R_{FMout}		50		kΩ
AM rejection ratio	m = 30% Pins 9 and 14	AM_{rr}		25		dB
Maximum AM input voltage	Pin 9	V_{AMmax}		90		dBµV
AM quiescent current	Pin 8	I_{AMout}	10	22	37	µA
Maximum AM current	Pin 8	$I_{AMoutmax}$		100		µA
Operational amplifier						
Gain bandwidth product	Pins 1, 2 and 16	f_t	3	4	6.5	MHz
Excess phase	Pins 1, 2 and 16	δ		80		degree
Open loop gain	Pins 1, 2 and 16	g_0	50	70	95	dB
Output voltage range	Pin 2	ΔV_{out}		1.55		V
Common mode input voltage	Pins 1 and 16	V_{in}	0.7		1.7	V
Input offset voltage	Pins 1 and 16	V_{os}	–2.5	0	+2.5	mV
Maximum output current	Pin 2	I_{out}			5	mA
Common mode rejection ratio	Pins 1 and 16	cmrr	65	85		dB
Total harmonic distortion	V_{in} < 300 mV, f = 33 kHz, unity gain circuit Pin 2	thd		1	3	%
Power supply rejection ratio	f = 50 Hz Pin 2	psrr	65	85		dB

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Clamping comparator						
Typical common mode input voltage range	Pin 2	Vcmvr	0.8		1.6	V
Maximum distortion voltage	V_{signal} = 100 mV, R+ = R– = 50 kΩ, C+ = C– = 200 nF, f_{disto} = 50 Hz, f_{signal} = 1 kHz Pin 2	V_{dmax}			200	mV
Output voltage	$V_2 > (V_6 + V_7)/2$ (10 kΩ load to V_{Ref}) Pin 5	V_{cout}	0	150	250	mV [1]
Output voltage	$V_2 < (V_6 + V_7)/2$ (10 kΩ load to V_{Ref}) Pin 5	V_{cout}		V_{Ref}		
Wake up circuit						
Minimum wake up level	Pin 9	V_{in}		40		dBµV [2]
Internal charging resistor	Pin 3	R_{int}		1.5		kΩ
Threshold voltage	Pin 3	V_{th}		1.6		V
Output switch current	Pin 10	I_{SW}	180	250	550	µA
Output switch voltage	Pin 10	V_{SW}			5.5	V [3]
External wake up resistor	Pins 3 and 13	R_{WU}	22			kΩ
External wake up capacitor	Pins 3 and 13	C_{WU}			10	µF
Hold time (± 30%)		t_h	$\approx 1.5 \times R_{WU} \times C_{WU}$			s [4]
Delay time (± 30%)		t_d	$\approx C_{WU} \times 0.75\ k\Omega$			s [4]

1) IC version with non-inverting comparator available: U4311B

2) Measured at Pin 9, referred to 330 Ω

3) Protected by a Z-diode, see figure 13

4) Valid for 0.1 µF ≤ C_{WU} ≤ 10 µF and 22 kΩ ≤ R_{WU} ≤ 680 kΩ

Application

The U4313B is well-suited to implement UHF remote control or data transmission systems, based on a low current superheterodyne receiver concept. SAW-devices may be used in the transmitter as well as in the receiver local oscillator. The front end should be a discrete circuit application with low-current UHF transistors like S822T or S852T from TEMIC TELEFUNKEN microelectronic GmbH. The frequency of the local oscillator can be determined either by coaxial resonators or SAW-devices. Due to large SAW-resonator tolerance IF-bandwidth – and in a FM-system additionally the discriminator amplitude characteristic (figure 28) – of 300 kHz or higher is proposed. As the circuit needs only 3.0 V supply voltage for operation, the front end may be a stacked design in order to achieve a total receiver current consumption of approximately 1 mA. Figure 29 shows a principle receiver concept diagram. The application notes ANT012, ANT013 and ANT015 contain more detailed information on complete RF links.

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The 10.7 MHz IF-signal from the front end passes the integrated IF-amplifier which operates for amplitude- or frequency-modulated signals to either a logarithmic AM-demodulator which was implemented to avoid settling time problems effected by use of an automatic gain control system or a quadrature detector for FM. A data shaping filter – advantageously realized with the internal high performance operational-amplifier – reduces system bandwidth to an optimized compromise regarding transmission distance and data recognition. Thus an optimal bit error rate can be achieved without any further active component.

The comparator connected to the output of the filter has a level-dependent hysteresis and clamps its reference voltage to the signal minimum and maximum peaks as described later.

Without IF-input signal – in the normal mode only the IF-amplifier and the AM demodulator which operates as a level strength indicator are activated. If the level of the IF signal increases, the whole circuitry is turned on by the wake-up circuit. This signal is externally available at pin 10 and can be used to wake up a microcontroller. After an adjustable reset time, determined by the monoflop time constant, the integrated circuit rests down to the sleep mode. In this case typically 1 mA supply current is required. An external resistor matched at pin 3 to ground blocks the wake-up circuit and gives fully function at lower IF-level as to recognize in figures 24 and 27, but supply current increases up to typically 2.8 mA.

Function of the clamping comparator

The output signal of the operational amplifier is fed to the input of the inverting comparator and two peak detectors (Q1 and Q2, figure 3). Their time constants are distinguished by RC+ and RC–. The components value must be adapted to the transmission code. The time constant should be large compared to the bit-rate for optimized noise and hum suppression. To compensate the input transistors base-emitter-voltage differences these two signals are buffered by Q3 and Q4. The mean value is used as comparator threshold, the difference of the peak values controls the hysteresis. This clamping comparator works as a data regenerator.

Another version of the IC, with a non-inverting clamping comparator, is also available (U4311B). Therefore the operational amplifier can be used either as a non-inverting or an inverting filter without the need of any additional components.

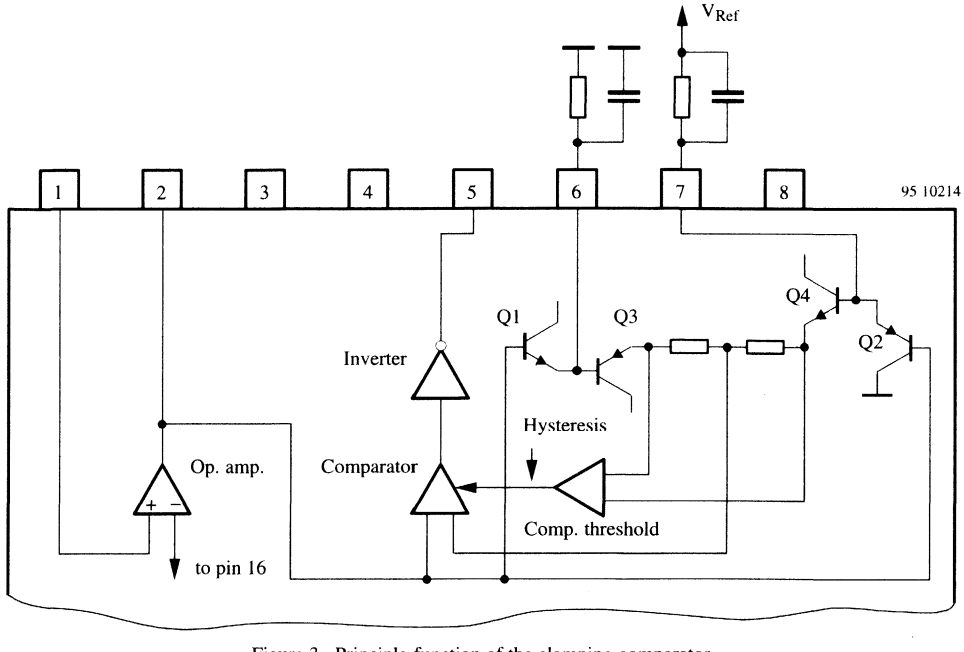


Figure 3. Principle function of the clamping comparator

Internal Pin Circuitry

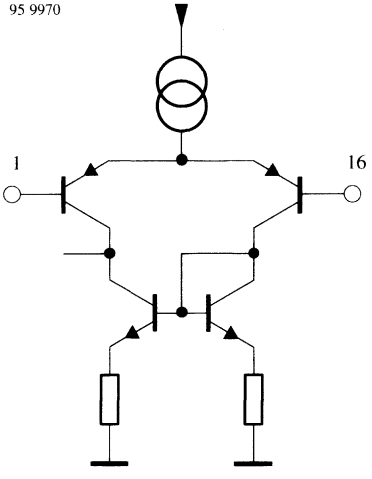


Figure 4. Pin 1 OP_{in+}

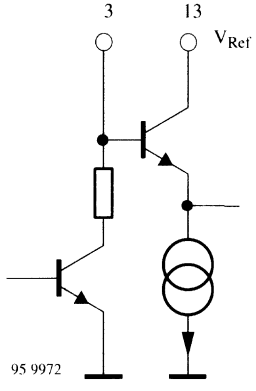


Figure 6. Pin 3 RC_{wake}

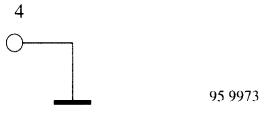


Figure 7. Pin 4 GND2

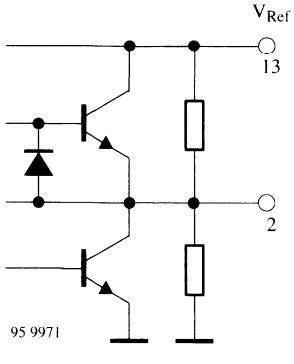


Figure 5. Pin 2 OP_{out}

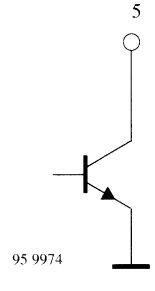


Figure 8. Pin 5 $Comp_{out}$

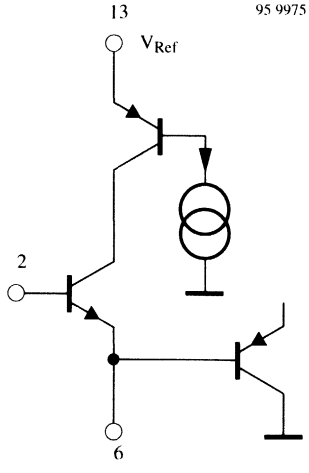


Figure 9. Pin 6 RC–

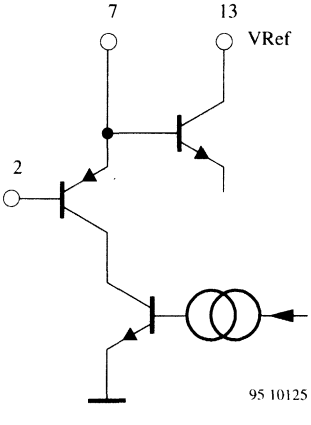


Figure 10. Pin 7 RC+

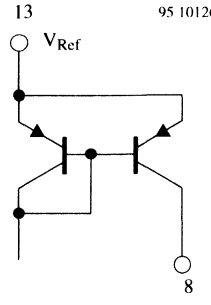


Figure 11. Pin 8 AM_{out}

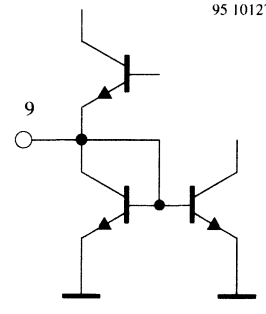


Figure 12. Pin 9 IF_{in}

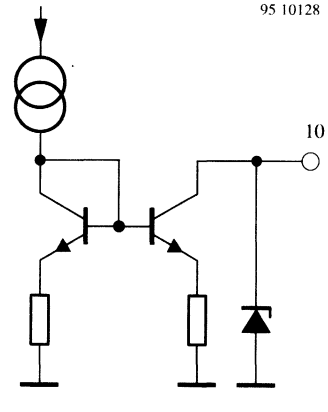


Figure 13. Pin 10 SW_{out}

Figure 14. Pin 11 GND1

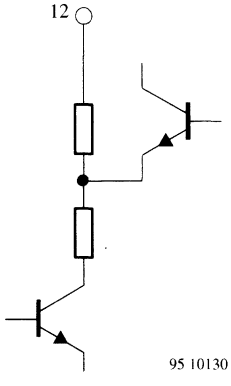


Figure 15. Pin 12 Discr

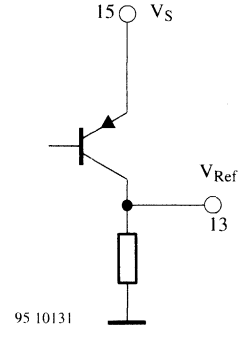


Figure 16. Pin 13 V_{Ref}

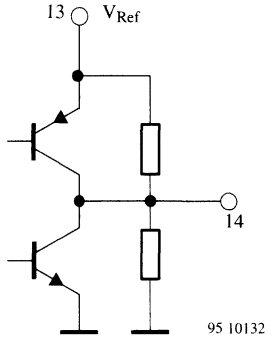


Figure 17. Pin 14 FM_{out}

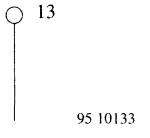


Figure 18. Pin 15 V_S

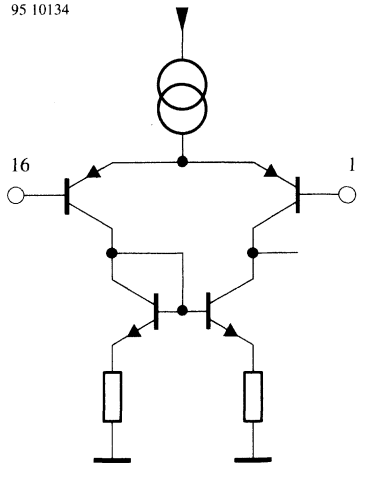


Figure 19. Pin 16 OP_{in-}

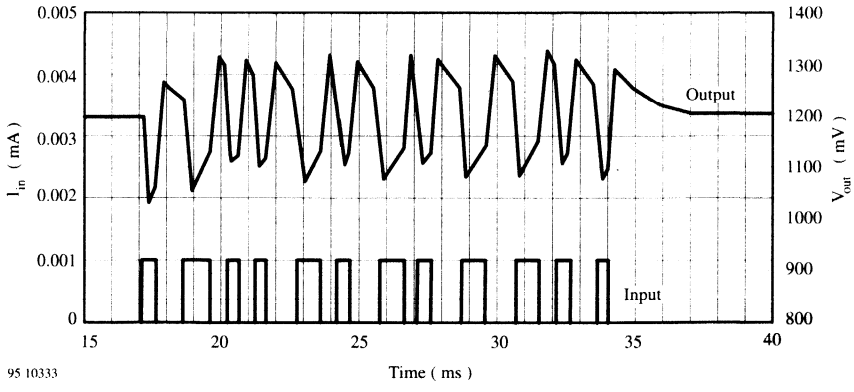


Figure 20. Time domain response of 2 kHz Bessel low pass data filter

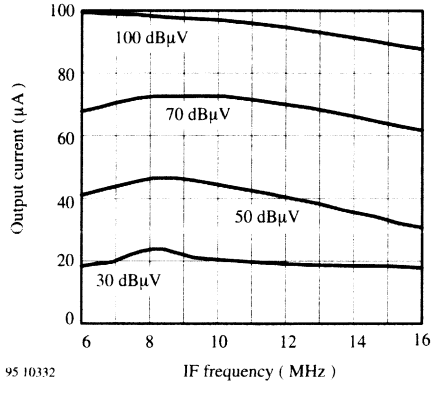


Figure 21. IF-frequency response

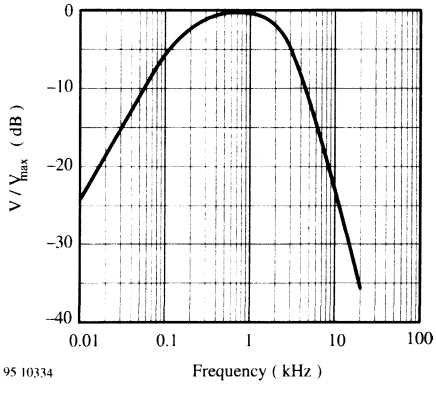


Figure 22. Frequency response of 2 kHz Bessel low pass data filter

Data Recovering Filter

The test circuit in figures 23 and 26 includes an example of a data recovering filter realized with the components R_1, R_2, C_1, C_2, C_3. It is of a second order Bessel type with low pass characteristic, a 3 dB cut-off frequency of 2 kHz and an additional high pass characteristic for suppressing dc and low frequency ac components. Simulation of time domain and frequency response is drawn in figures 20 and 22. This filter gives a typical application of a 1 kBaud Manchester code amplitude modulated transmission.

The capacitor C_2 is responsible for the high pass cut-off frequency. For a correct pulse response this high pass cut-off frequency should be as low as possible. Figure 20 shows the transient response and the influence of the dc component. The first pulses might be wrong if the high pass cut-off frequency is too low. For this reason some burst bits must be transmitted before the real data transmission starts. On the other hand, if the cut-off frequency is too high, you might get in trouble with roof shaping of the rectangle pulses at the operational amplifier output.

The low pass cut-off frequency and the maximum transimpedance V_{out}/I_{in} are distinguished by the further external elements. Careful design of the data filter gives optimized transmission range. For designing other filter parameters look for filter design handbooks or programs or request TEMIC TELEFUNKEN microelectronic GmbH for support. Some proposals can be found in the application notes ANT012, ANT013 and ANT015.

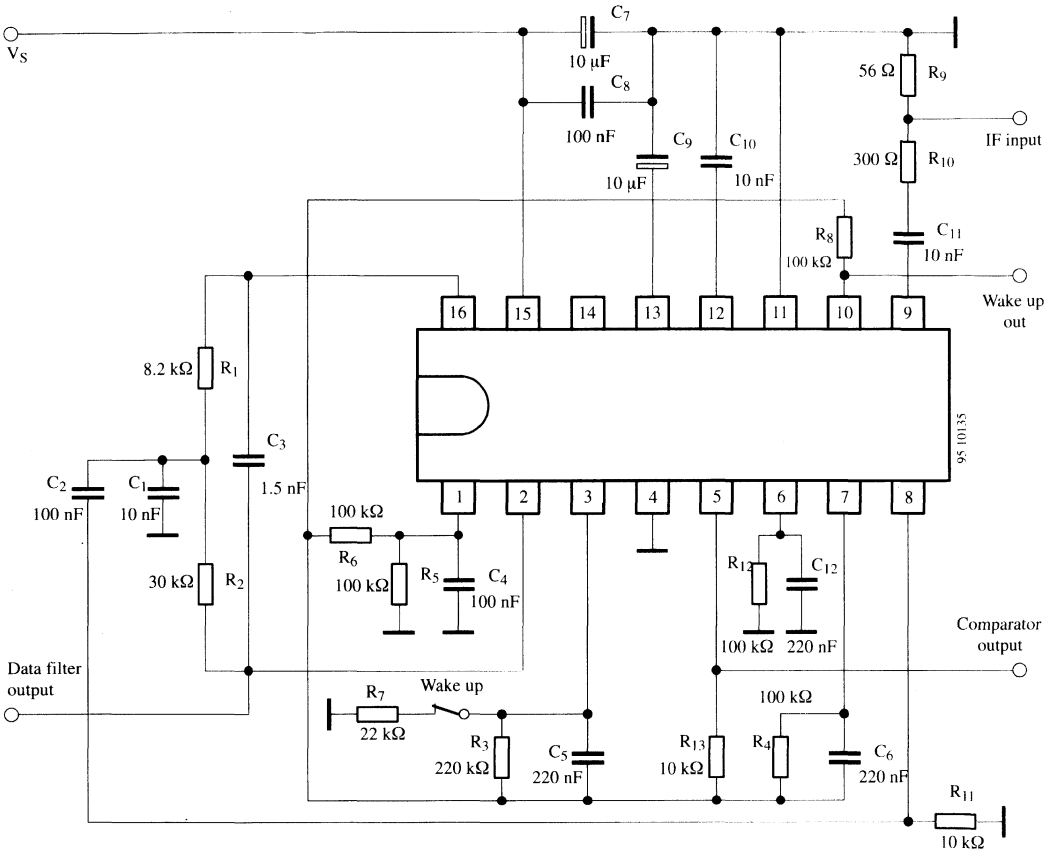


Figure 23. AM test circuit with 2 kHz Bessel low pass data filter

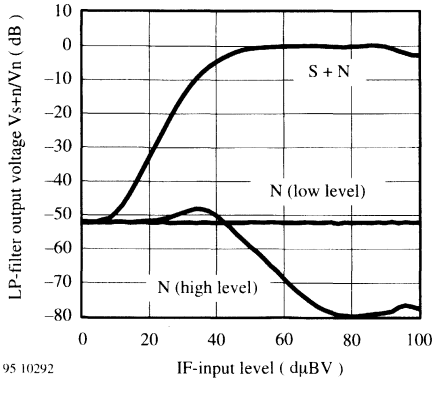


Figure 24. Signal to noise ratio AM

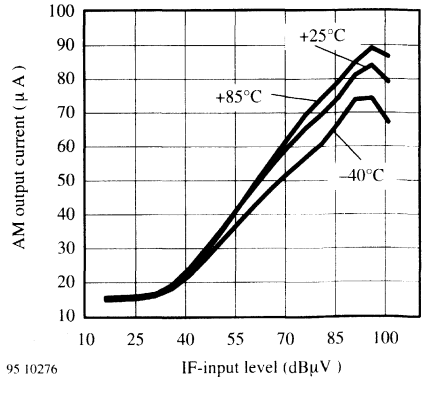


Figure 25. AM-demodulator characteristic vs. temperature

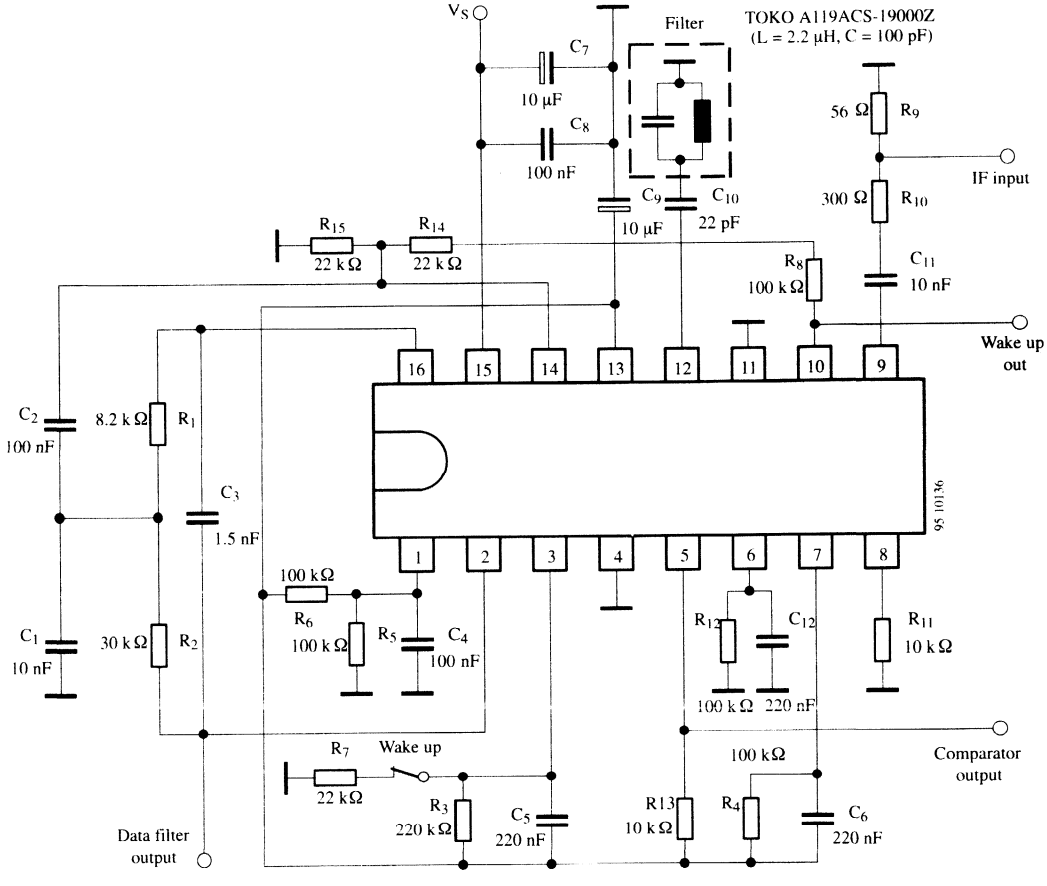


Figure 26. FM test circuit with 2 kHz Bessel low pass data filter

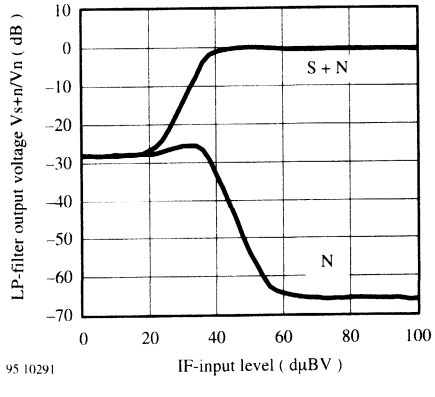


Figure 27. Signal to noise ratio FM; deviation 22.5 kHz

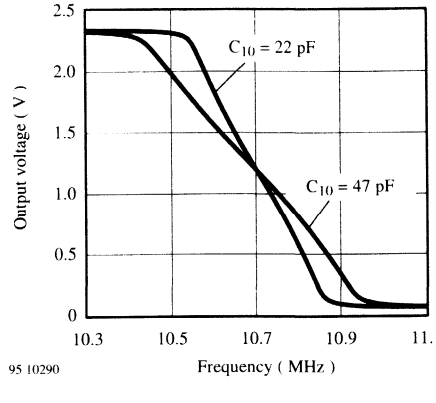


Figure 28. FM-discriminator characteristic

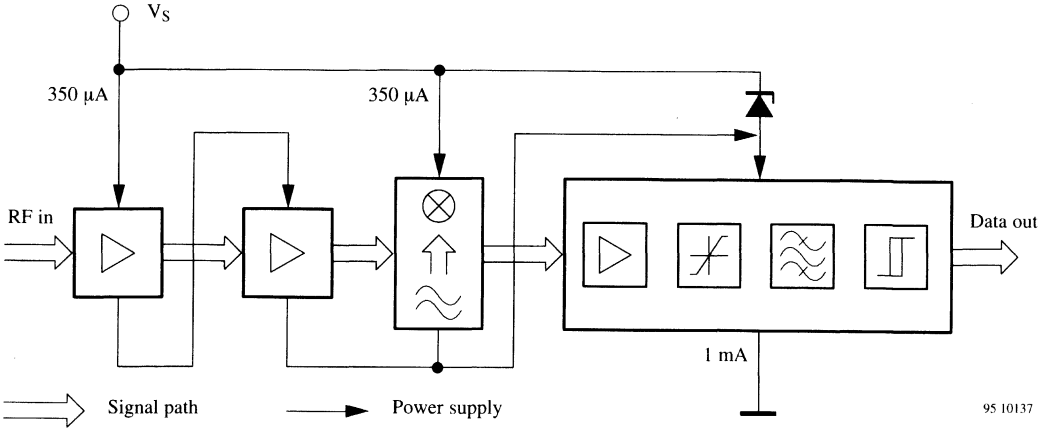


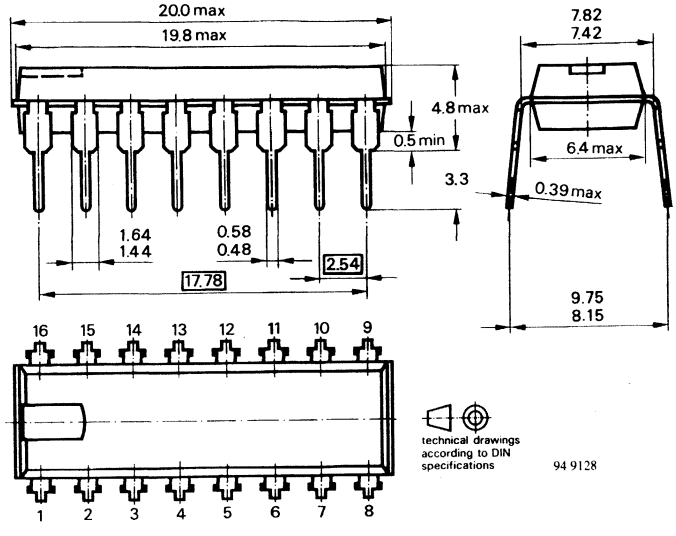
Figure 29. Principle diagram UHF remote control receiver

Ordering Information

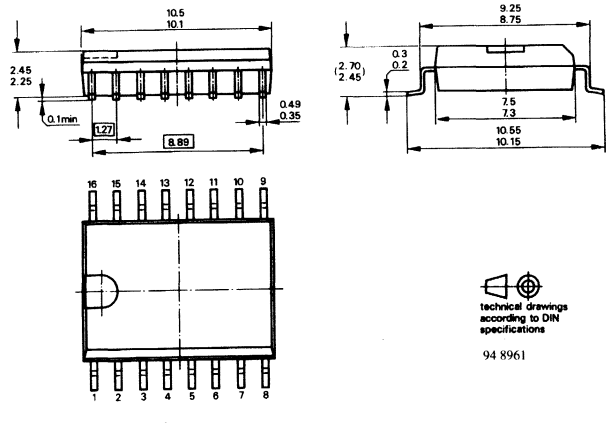
Extended Type Number	Package	Remarks
U4313B-A	DIP16	
U4313B-AFL	SO16L	

Dimensions in mm

Package DIP16



Package SO16L



Logarithmic AM Demodulator / RSSI

Description

The U4314B is a monolithic Integrated Circuit in bipolar technology for low current super-heterodyne receivers. It can be used as a logarithmic **R**eceived **S**ignal **S**trength **I**ndicator (RSSI) or as a logarithmic AM demodulator. Its bandwidth is optimized for intermediate frequencies of 9 to 10.7 MHz (see figure 9).

Its low current consumption and wide power supply voltage range make this IC predestined to add a temperature compensated field strength indication to new or existing receiver or instrumentation designs, missing such a function.

It can also be used as a logarithmic AM demodulator. Its dynamic range in excess of 60 dB (see figure 10) supports a receiver design without the need of an automatic gain control (AGC). The usable data rate is up to several hundred kBauds. Typical applications are keyless entry and alarm systems for cars and buildings.

The U4314B supports a superhet receiver design with less than 1 mA total current consumption, which is a peremptory requirement claimed by international car manufacturers. As this IC needs only 3.0 V supply voltage, the front end may be a stacked design in order to reach this extremely low total receiver current consumption.

A proposal for a discrete RF front end with a surface acoustic wave (SAW) resonator based local oscillator special low current UHF-transistors like S822T or S852T can be found in the application notes ANT012 and ANT013.

Features

- Logarithmic RSSI / AM demodulator output
- Sensitive IF-amplifier for 10.7 MHz operating frequency
- Usable for ASK data systems up to several hundred kBauds
- Extreme low current consumption typically 0.8 mA
- Wide power supply voltage range 3 to 12 V
- Temperature compensated reference voltage of 2.4 V externally available
- Only one additional part (capacitor) necessary
- ESD hardened

Block diagram

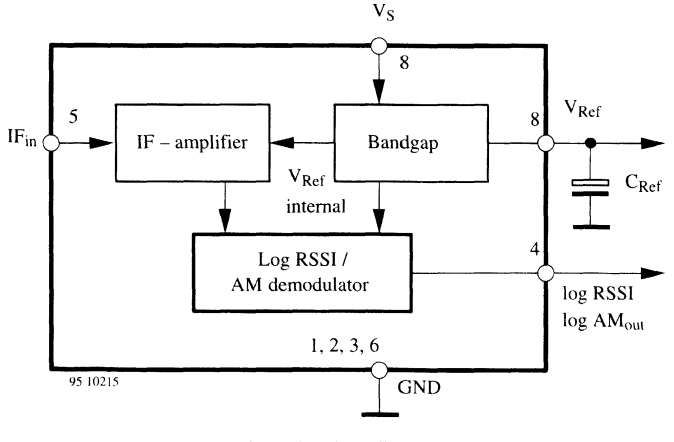


Figure 1. Block diagram

Pin Description

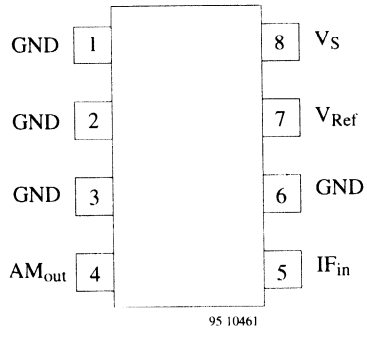


Figure 2. Pin description

Pin	Symbol	Function
1, 2, 3, 6	GND	Ground
4	AM_{out}	RSSI / AM current output
5	IF_{in}	IF input
7	V_{Ref}	Reference voltage
8	V_S	Supply voltage

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_S	13	V
Power dissipation at T_{amb} = 85°C	P_{tot}	220	mW
Junction temperature	T_j	125	°C
Ambient temperature	T_{amb}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	180	K/W

Electrical Characteristics

V_S = 5 V, T_{amb} = 25°C, f_{in} = 10.7 MHz unless otherwise specified. Test circuit see figure 8. IF voltage levels are referred to the input of the matching network and therefore approximately 5.6 dB higher than referred to Pin 5.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Characteristics						
Supply voltage range	Pin 8	V_S	3		12	V
Supply current	Pin 8	I_S		0.8	1.25	mA
Bandgap						
Regulated voltage (without external load)	Pin 7	V_{ref}	2.3	2.4	2.5	V
Source resistance	Pin 7	R_{ref}		2	5	Ω
Output current	Pin 7	I_{ref}			5	mA
External capacitor	Pin 7	C_{ref}		4.7		µF
Power supply rejection ratio	f = 50 Hz Pin 7	psrr		60		dB
IF amplifier						
Input resistance	Pin 5	R_{in}	200	330	650	Ω
Input capacitance	Pin 5	C_{in}		5		pF
–3 dB limiting point	Pin 5	V_{IFin}	26	36	46	dBµV
Maximum AM input voltage	Pin 5	$V_{IFinmax}$		96		dBµV
AM_{out} quiescent current	R_{load} = 10 kΩ Pin 4	I_{AMout}	10	22	38	µA
Maximum AM_{out} current	V_{IFin} = 96 dBµV, R_{load} = 10 kΩ Pin 4	$I_{AMoutmax}$	75	105	125	µA

Circuit Description

General functions

The integrated circuit U4314B includes the following functions: IF-amplifier, logarithmic RSSI / AM demodulator and voltage-regulator.

The 10.7 MHz IF-signal from the front end passes the integrated IF-amplifier which operates to a logarithmic RSSI / AM-demodulator. A logarithmic demodulator was implemented to avoid settling time problems effected by use of an AGC. The temperature compensated reference voltage of 2.4 V is externally available. The value of the external blocking capacitor can be adapted to the maximum expected load current out of the voltage regulator. The total supply current is typically 0.8 mA plus this load current.

Figure 3. Pin 1, 2, 3, 6 GND

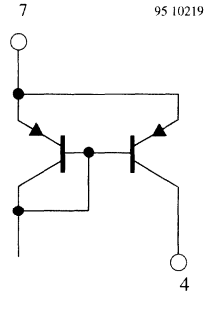


Figure 4. Pin 4 AM_{out}

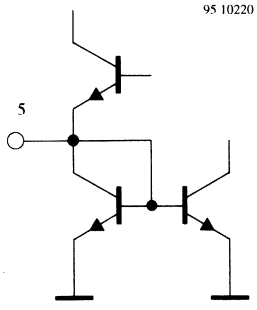


Figure 5. Pin 5 IF_{in}

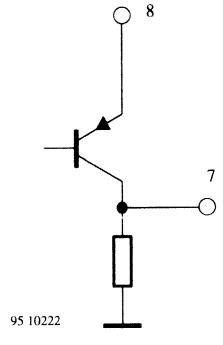


Figure 6. Pin 7 V_{Ref}

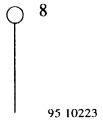


Figure 7. Pin 8 V_S

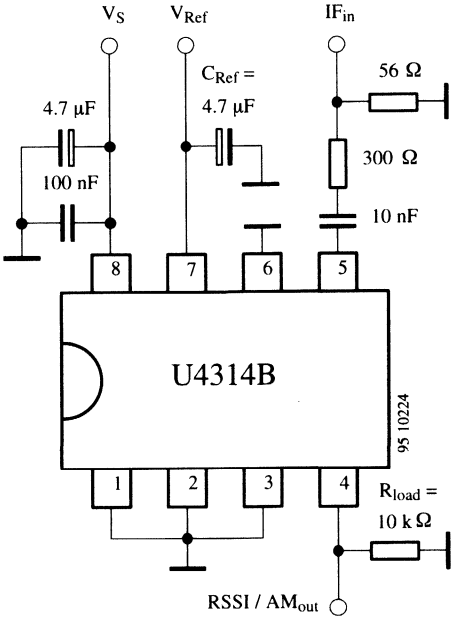


Figure 8. Test circuit

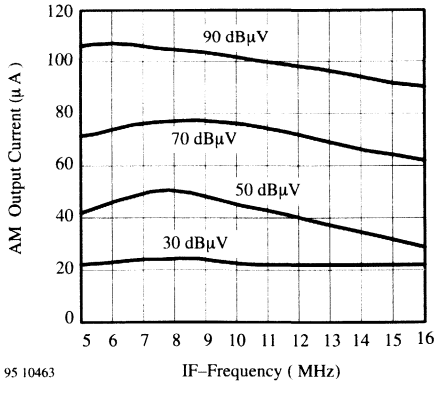


Figure 9. IF-Frequency response

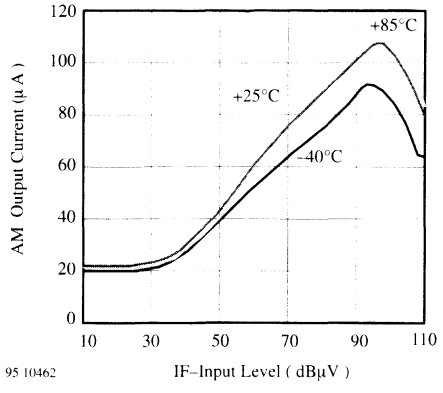


Figure 10. AM-demodulator characteristic (f_{in} = 10.7 MHz)

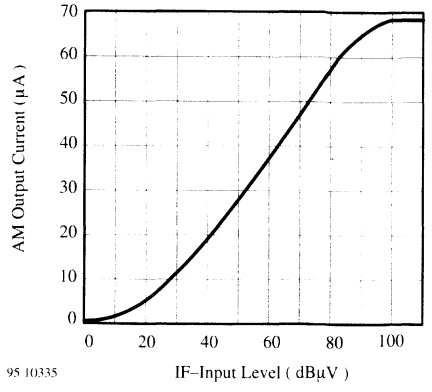


Figure 11. IAM_{out} of U4314B in the application circuit of figure 12 (f_{in} = 107 MHz)

The following circuit is a mere proposal, how to improve sensitivity and extend the dynamic range of U4314B to more than 90 dB. However in most applications the basic dynamic range of more than 60 dB is sufficient. TEMIC TELEFUNKEN microelectronic GmbH makes no representation that the use of this circuit will not refringe on existing or future patents and no responsibility for the use of the information contained herein is assumed. This circuit is neither optimized concerning tolerances of the components nor tested versus temperature. It should work with a single supply voltage of 3 to 12 V. A npn transistor array CA3045 or similar is used. At least four transistors are needed to realize two current mirrors and the fifth acts as a preamplifier. The variable resistor P_1 is used to compensate the quiescent current of the logarithmic demodulator output and may be replaced by a fixed resistor (typ. 3.3 kΩ). The total supply current depends on the IF-input level and varies between 2 and 7 mA. It is mainly determined by the current through the PIN diode. We recommend to use the BA679S PIN diode available from TEMIC TELEFUNKEN microelectronic GmbH. The input impedance of this application circuit is approximately 1.5 kΩ || 13 pF.

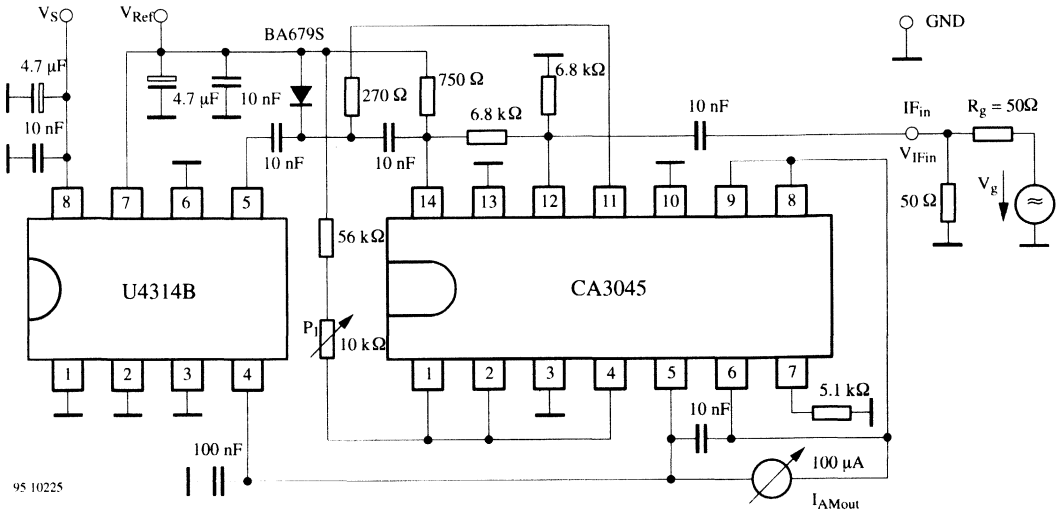


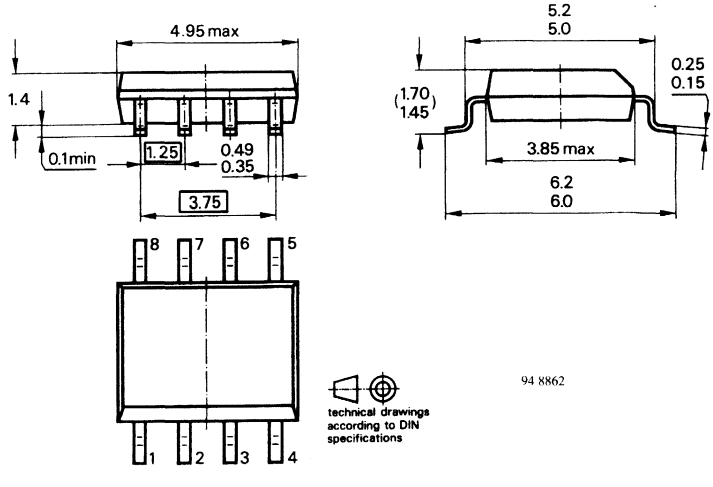
Figure 12. Application circuit with a dynamic range in excess of 90 dB

Ordering Information

Extended Type Number	Package	Remarks
U4314B-AFP	SO8	

Dimensions in mm

Package SO8



Reader-IC for Immobilizers

Description

The U2270B is a bipolar integrated circuit which implements all important functions for immobilizer and identification systems. The IC incorporates the required circuitry for the energy transfer to the transponder, like on chip power supply, oscillator and a powerful reader coil driver. It also includes all signal processing circuits that are necessary to form the small input signal into a microcomputer output information.

Features

- Power supply: 5 V or battery voltage (7 V to 14 V)
- Tuning capability
- Microcontroller compatible
- Special coil driver function: common mode or differential mode
- Power supply output for microcontroller
- Low power consumption in standby mode

Applications

- Car immobilizer
- Access control
- Animal identification
- Access control combined with credit card

Case: SO 16 U2270B-FP

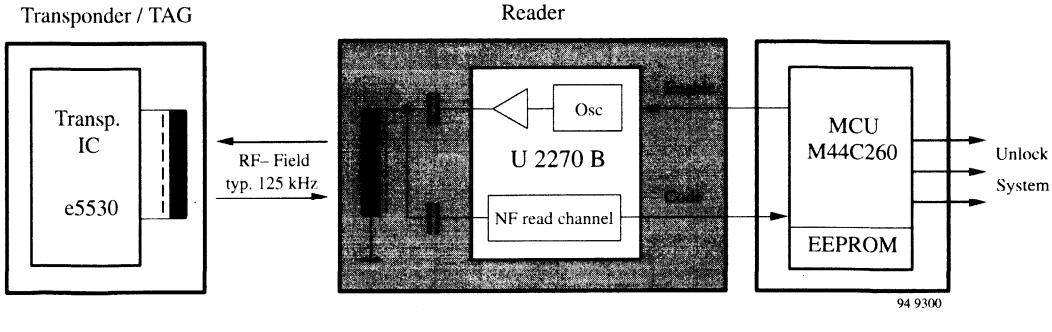


Figure 1.

Pin Description

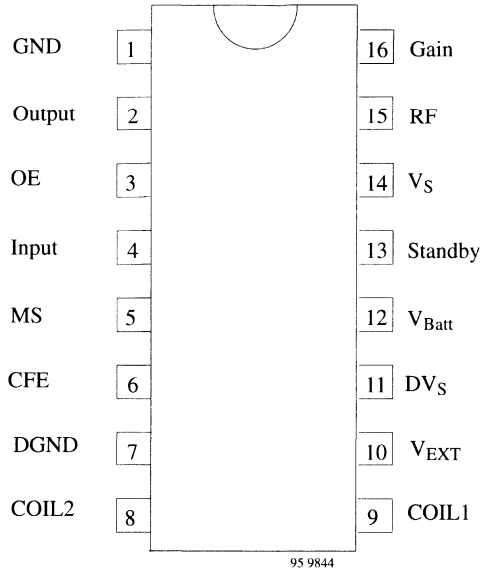


Figure 2. Pinning

Pin	Symbol	Function
1	GND	Ground
2	Output	Data output
3	OE	Data output enable
4	Input	Data input
5	MS	Mode select coil 1: Common mode / Differential mode
6	CFE	Carrier frequency enable
7	DGND	Driver ground
8	COIL 2	Reader coil driver 2
9	COIL 1	Reader coil driver 1
10	V_{EXT}	External power supply
11	DV_S	Driver supply voltage
12	V_{Batt}	Battery voltage
13	Standby	Standby input
14	V_S	Internal power supply (5 V)
15	RF	Frequency adjustment
16	Gain	Gain control

Block Diagram

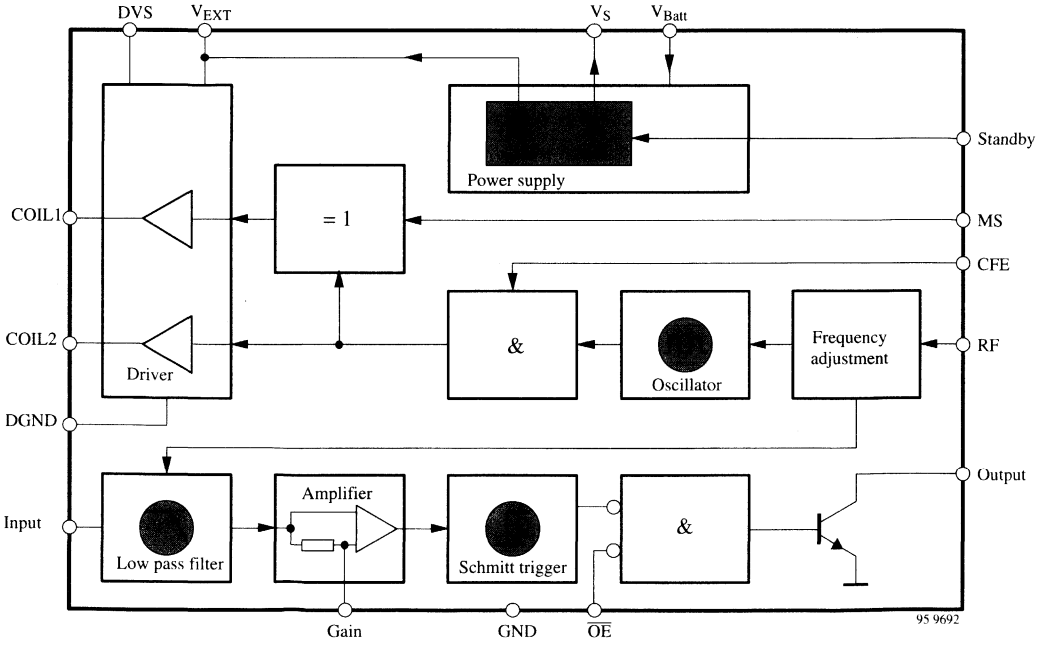


Figure 3.

Functional Description

Power Supply (PS)

The U2270B can be operated from a single 5 V supply rail or from the 12 V battery voltage of a vehicle. The 12 V supply capability is achieved via the on chip power supply (see figure 3). The power supply provides two different output voltages, V_S and V_{EXT}.

V_S is the internal power supply voltage except of that for the driver circuit. Pin V_S is used to connect a block capacitor. V_S can be switched off by the Pin Standby. In the standby mode, the chip's power consumption is very low. V_{EXT} is the supply voltage of the antenna's predriver. This voltage can also be used to operate external circuits i.e. a microcontroller. In conjunction with an external NPN transistor, it also establishes the supply voltage of the reader coil driver, DVS.

There are mainly 3 different possibilities to power the different systems of the reader IC.

1. One Rail Operation

All internal circuits are operated from one 5 V power rail (refer to figure 1). V_S ,V_{EXT} and DV_S serve as inputs in that case. V_{Batt} is not used, but should also be connected to that supply rail.

2. Two Rail Operation

In that application, the driver voltage (DV_S) and the predriver supply (V_{EXT}) are operated at a higher voltage than the rest of the circuits, to obtain a higher magnetic field. V_S is connected to a 5 V supply, whereas the driver voltages can be as high as 8 V.

3. Battery Voltage Operation

Using this operation mode, V_S and V_{EXT} are generated by the internal power supply (refer to figure 2). V_{EXT} is an output voltage in that case and supplies the base of the external NPN transistor. The emitter of that transistor can deliver the current for the output stage of the antenna driver.

Oscillator Osc

The frequency of the on-chip oscillator is controlled by a current fed into the R_F input. An integrated compensation circuit ensures a widely temperature and supply voltage independent frequency which is selected by a fixed resistor between R_f (Pin 15) and V_S (Pin 14). For 125 kHz a resistor value of 110 kΩ is defined. For other frequencies use the following formula:

$$R_f = \frac{14375}{f_0\,[kHz]} - 5\ k\Omega$$

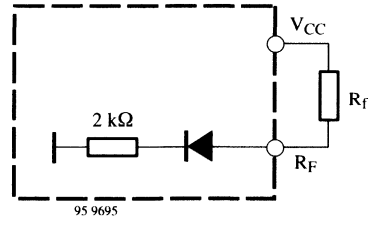


Figure 4. Equivalent circuit of pin R_F

Filter (LPF)

The full integrated low-pass filter (4th order butterworth) removes the remaining carrier signal and high frequency disturbances after demodulation. The upper cut-off frequency of the LPF depends on the selected oscillator frequency. The typical value is f(osc)/18. That means data rates up to fosc/25 are possible if biphase encoding is used.

A high pass filter results from the capacitive coupling at the input (Pin 4) shown in figure 5. The input voltage swing is limited at 2 V_{pp}. For frequency response calculation the impedances of the signal source and LPF input (typical 220 kΩ) have to be considered.

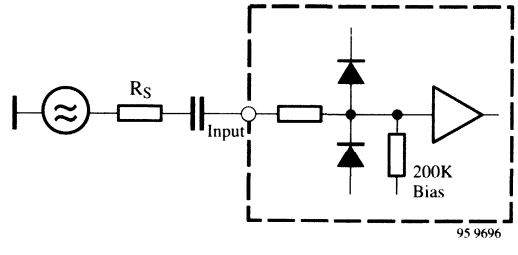


Figure 5. Equivalent circuit of Pin Input

Amplifier (AMP)

The differential amplifier basically has a fixed gain. The Gain pin is used for dc decoupling and to set the gain to a lower value by an additional resistor (R_{Gain}). The lower cut-off frequency of the decoupling circuit and the gain are as follows:

$$G = 30\ \frac{R_i}{R_i + R_{Gain}}$$

$$f_{cut} = \frac{1}{2\ \pi\ C_{Gain}\ (\ R_i + R_{Gain})}$$

The value of the internal resistor R_i can be assumed to 2.5 kΩ.

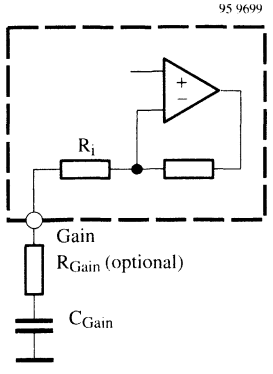


Figure 6. Equivalent circuit of pin GAIN

Schmitt-Trigger

Finally the signal is processed by a schmitt-trigger to suppress noise and to make it µC compatible. The hysteresis is 100 mV symmetrically to the DC operation point. The open collector output is enabled by a low level at OE (Pin 3).

Driver (DRV)

The driver supplies the reader coil with the appropriate energy. The circuits consists of two independent output stages. This output stages can be operated in two different modes. In the common mode, the outputs of the stages are in phase. In this mode, the outputs can be interconnected, to achieve a high current output capability. Using the differential mode, the output voltages are in antiphase. In this way, the reader antenna is driven with a higher voltage, having a lower output current capability. These functions are controlled by two digital inputs (MS, CFE, refer to function list). The equivalent circuit of the driver is shown in figure 3.

Function List

MS low	common mode
MS high	differential mode
CFE low	carrier disabled
CFE high	carrier active
OE low	output enabled
OE high	output disabled
Standby low	standby mode
Standby high	IC active

Absolute Maximum Ratings

All voltages are referred to GND (pins 1 and 7).

Parameters/Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Operating voltage	Pin 12	V_{Batt}	V_S		14	V
Operating voltage	Pins 10 and 14	V_S, V_{EXT}	–0.3		8	V
Range of all input and output voltages Pins 2, 3, 4, 5, 6, 8, 9, 13, 15 and 16			–0.3		V_S+0.3	V
Output current	Pin 10	I_{EXT}			10	mA
Output current	Pin 2	I_{OUT}			10	mA
Driver output current	Pins 8 and 9	I_{coil}			200	mA
Power dissipation	SO 16	P_{tot}			380	mW
Junction temperature		T_{imax}			150	°C
Storage temperature		T_{stg}	–55		125	°C
Ambient temperature		T_{amb}	–40		105	°C

Maximum Thermal Resistance

Parameters/Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance	SO 16	R_{thJA}			120	K/W

Operating Range

All voltages are referred to GND (pins 1 and 7)

Parameters/Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Operating voltage	Pin 12	V_{Batt}	7	12	14	V
Operating voltage	Pin 14	V_S	4.5	5.3	6.0	V
Operating voltage	Pin 10 Pin 11	V_{EXT} DV_S	4.5		8	
Carrier frequency		f_{osc}	100	125	150	kHz

Electrical Characteristics

Test conditions (unless otherwise specified): V_{Batt} = 12 V, T_{amb} = 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Data output – collector emitter saturation voltage	Pin 2 I_{out} = 5 mA	V_{CEsat}			400	mV
Data output enable – low level input voltage – high level input voltage	Pin 3	V_{il} V_{ih}	 2.4		0.8	V V
Data input – low level input voltage – high level input voltage input resistance – input sensitivity	Pin 4 f = 3 kHz (squarewave) gain capacitor = 100 nF	 V_{il} V_{ih} R_{in} 	 2 10	 220 	 3.8 	 V V kΩ mV
Driver polarity mode – low level input voltage – high level input voltage	Pin 5	V_{il} V_{ih}	 2.4		0.2	V V
Carrier frequency enable – low level input voltage – high level input voltage	Pin 6	V_{il} V_{ih}	 3.0		0.8	V V
Operating current	Pin 14	I_S		1.4		mA
Standby current	Pin 12	I_{St}	16	28	40	µA
Supply voltage	Pin 14	V_S	4.5	5.3	6	V
Driver output voltage	I_L = ±100 mA Pin 7	V_{DRV}	3.3	4.0		V_{PP}
Vext – Output voltage – Output current – Standby output current	Pin 10 IC active standby mode	 V_{EXT} I_{EXT} I_{osc}	 5.0 	 5.5 1	 6.0 3.5 1.2	 V mA mA
Standby input – low level input voltage – high level input voltage	Pin 13	V_{il} V_{ih}	 2.5		0.8	V V

Electrical Characteristics

Test conditions (unless otherwise specified): V_{Batt} = 12 V, T_{amb} = 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Oscillator – Carrier frequency	RF-resistor = 110 kΩ (application 2)	f_0	123	125	127	kHz
Low pass filter – Cut off frequency	Carrier freq. = 125 kHz	f_{cut}		7		kHz
Amplifier – Gain	Gain capacitor = 100 nF f = 3 kHz		25	30	35	
Schmitt trigger – Hysteresis voltage				100		mV

Application 1

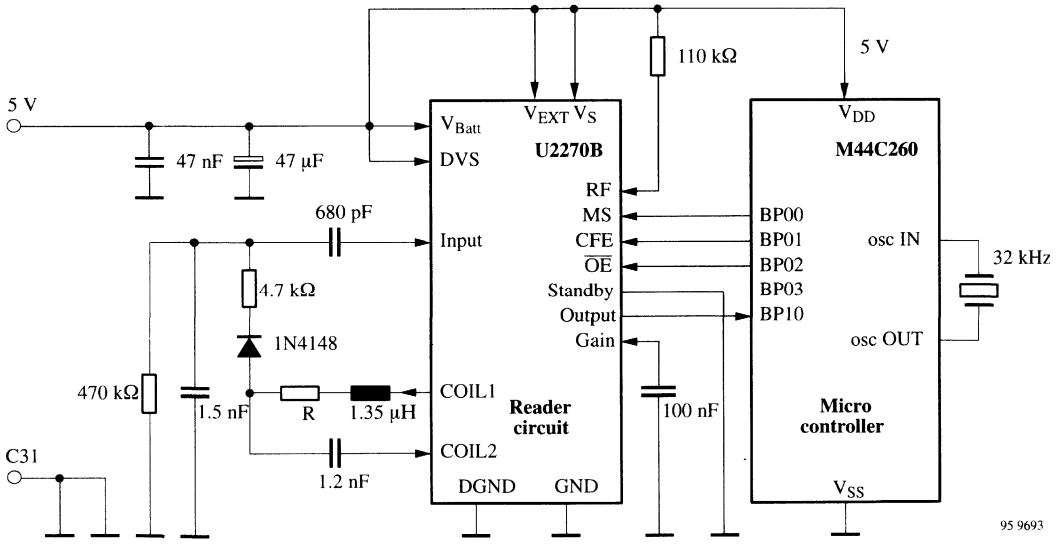


Figure 7.

Application 2

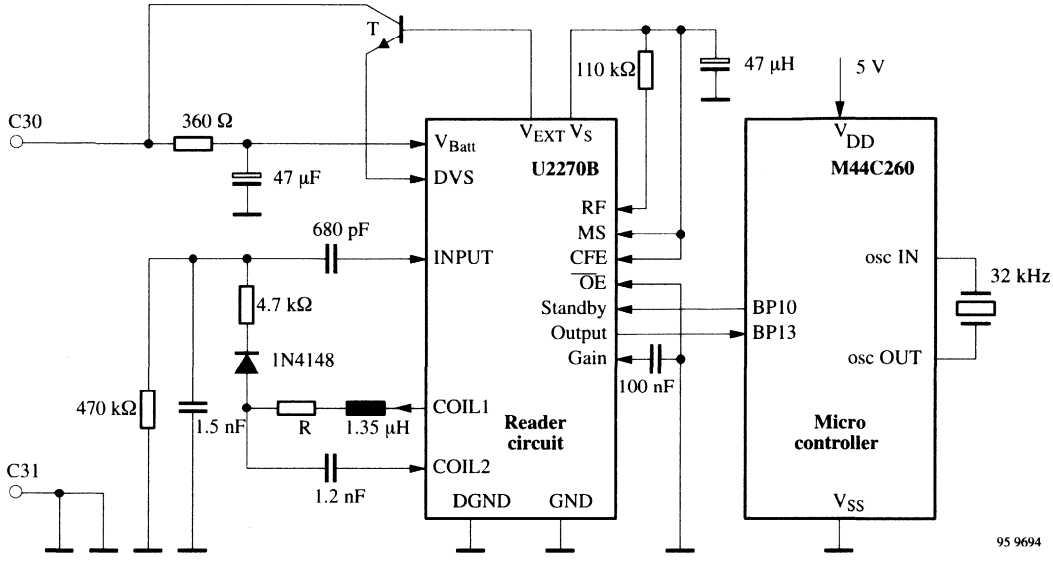
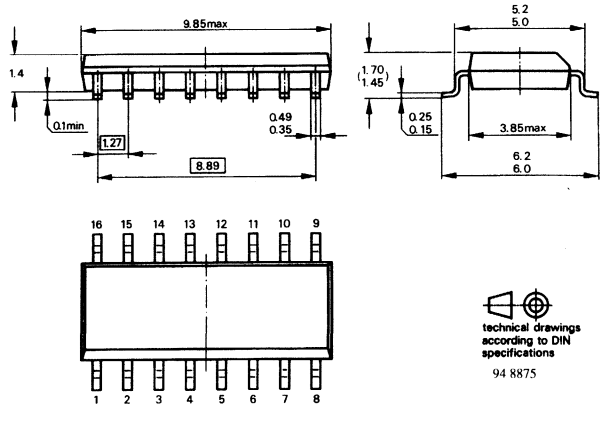


Figure 8.

Dimensions in mm

Package: SO 16



128 Bit IDIC® for Radio Frequency Identification

IDIC® stands for **ID**entification **I**ntegrated **C**ircuit and is a trademark of EUROSIL electronic GmbH.

Description

The e5530 is part of a closed coupled identification system. It receives power from an RF transmitter which is coupled inductively to the IDIC®. The frequency is typically 100 to 450 kHz. Receiving RF, the IDIC® responds with a data stream by damping the incoming RF via an internal load. This damping-in-turn can be detected by the interrogator. The identifying data are stored in a 128 bit PROM on the e5530, realized as an array of laser-programmable fuses. The logic block diagram for the e5530 is shown in figure 2. The data are output bit-serially as a code of length 128, 96, 64 or 32 bits. The chips are factory-programmed with a unique code.

Features

- Low power, low voltage CMOS
- Rectifier, voltage limiter, clock extraction on-chip (no battery)
- Small size
- Factory laser programmable ROM
- Operating temperature range –40 to +125°C
- **R**adio **F**requency (RF): 100 to 450 kHz
- Transmission options
  Code length: 128, 96, 64, 32 bits
  Bitrate [bit/s]: RF/8,RF/16, RF/32, RF/40, RF/50, RF/64, RF/80, RF/100, RF/128, RF/256
  Modulation: FSK, PSK, BIPH, Manchester BIPH-FSK

Application

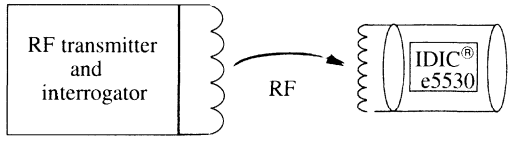


Figure 1.

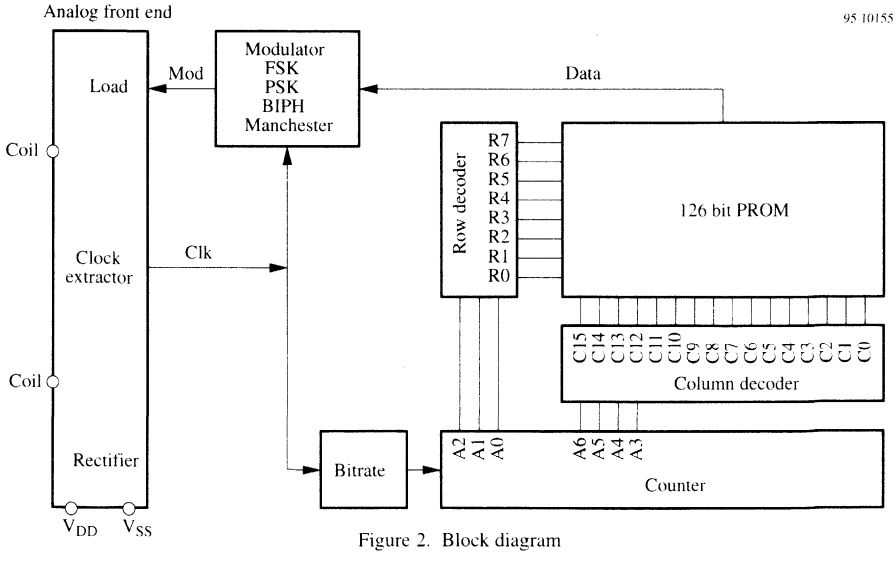


Figure 2. Block diagram

Functional Description

Read Operation

Once the IC detects the incoming RF, the IC repetively reads out the code data as long as the RF signal is applied. The transition from the last bit to bit 1 of the next sequence occurs without interruption. Data is transmitted by alternating damping of the incoming RF via a load. Different kinds of modulation and bitrates are optionally available.

Rectifier

For internal power supply, an on-chip bridge rectifier is used which consists of two diodes and two n-channel transistors. A Zener diode, which protects the circuit against overvoltage on the coil inputs, and a smoothing capacitor for the internal supply are also provided.

Damping Load

Incoming RF will be damped by the power consumption of the IC itself and by an internal load, which is controlled by the modulator. The loads are p-channel transistors connected between V_{DD} and the coil inputs. The layout includes metal mask options for the load circuit: single-side, double-side and alternate-side modulation.

Modulator

One of four methods of modulation can be selected by fuses. The timing diagram is shown in figure 3.

FSK

Logical "1" and "0" are distinguished via different frequencies of damping. The frequency for "1" is the RF divided by 10, a "0" divides by 8.

PSK

A logical "1" causes (at the end of the bit period) a 180° phase shift on the carrier frequency, while a logical "0" causes no phase shift. The carrier frequency is RF/2.

BIPH

Logical "1" produces a signal which is the same as the bitclock and a logical "0" produces a signal of twice the bitclock period.

Manchester

A logical "1" causes a positive edge in the middle of a bit period, while a logical "0" causes negative edge.

A combination of BIPH- and FSK-modulation is also optionally available. The available combinations between the modulation types and the bitrates are shown in table "Transmission Options".

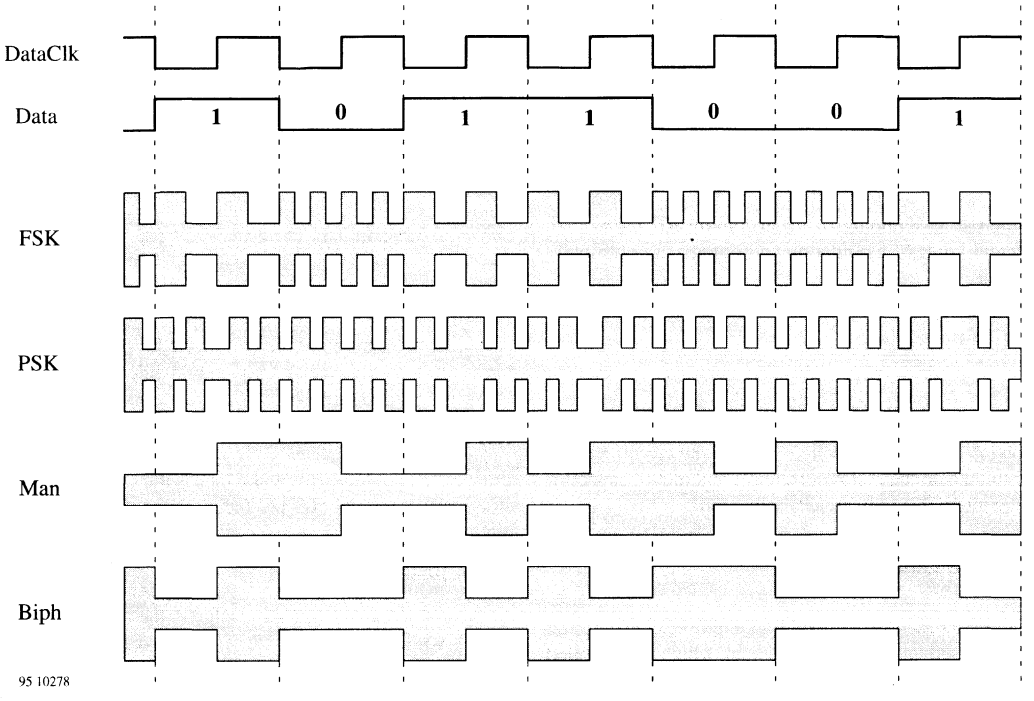


Figure 3. Timing diagram for modulation options

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Maximum current into Coil1 and Coil2		10	mA
Maximum power dissipation (dice)		100	mW*
Maximum ambient air temperature with voltage applied		–40 to +125	°C
Storage temperature		–65 to +150	°C

* Free-air condition. Time of application: 1 s
Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. Functional operation of the device at these conditions is not imlied.

Operating Characteristics

T_{AMB} = 25°C, reference terminal is V_{DD}, operating voltage $V_{DD} - V_{SS}$ = 3 V dc, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ. *	Max.	Unit
Operating voltage	Condition for logic test	V_{SS}	–1.5		–5.0	V_{DC}
Operating temperature		T_{AMB}	–40		125	°C
Input frequency (RF)		f_{CLK}	100		450	kHz
Operating currentin	f_{CLK} = 125 kHz, V_{SS} = –2 V	I_{CC}		3		µA
Clamp voltage	I = 4 mA	V_{CL}	67		10	V

* Typical parameters represent the statistical mean values

Transmission Options

Modulation	Carrier Frequency (CF)	Bitrate (bps)
FSK	RF/8, RF/10	RF/32, RF/40, RF/50, RF/64, RF/80, RF/100, RF/128
PSK	RF/2	CF/4, 8, 16, 32
BIPH		RF/8, RF/16, RF/32, RF/64, RF/100, RF/128
Manchester		RF/8, RF/16, RF/32, RF/64, RF/100, RF/128

e5530GT

Glass Tube Transponder

Description

The e5530GT is part of a closed coupled identification system. It receives power from an RF transmitter (base station, reader) which is coupled inductively to the IDIC.

Receiving RF, the **ID**entification **IC** (IDIC®) is powered up and responds with a data stream by damping the incoming RF via an internal load. This damping-in-turn can be detected by the reader. The identifying data are stored in a Laser–ROM on the e5530, which is factory-programmed with a unique code.

The ID code and other features like bitrate and modulation method are programmed according to the customer's request.

Features

- Low power, low voltage CMOS IDIC®
- LC antenna tuned to 125 kHz ± 3%
- Needs only 6 A/m for correct operation
- Encapsulated in a tiny glass tube dimensions: 12.0 × ∅ 2.1 mm
- Contactless power supply
- Contactless read data transmission
- Up to 128 bits of factory-programmed ID code
- Several transmission options:
  Code length: 32, 64, 96, 128 bits
  Bitrate: RF/8, RF/16, RF/32, RF/40, RF/50 RF/64, RF/80, RF/100, RF/128
  Modulation: FSK, PSK, Manchester, Biphase

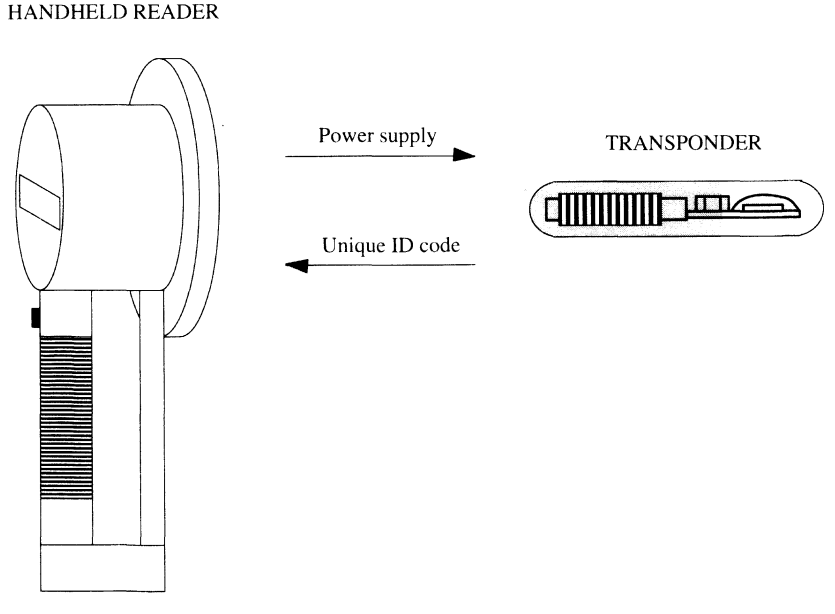


Figure 1. A transponder system example using the e5530GT

Functional Description

Supply

The e5530GT consists of a tuned coil and the e5530 IDIC®. This tuned coil has to be inductively coupled to the coil of the base station.

The base station coil generates a magnetic RF field, which induces a current at the transponder coil. At resonance frequency, several volts are available at the coil terminals. The IDIC® is powered by this energy.

Since the e5530 needs only some micro watt for correct operation, the transponder can operate in very weak magnetic fields.

Read

After power-up, the e5530 starts transmission of the ID code in the laser ROM.

Data transmission occurs by damping the incoming RF by an internal load. This load changing can be detected by the base station.

There are four modulation methods available.

FSK Modulation

A data '1' and a data '0' are represented as two different frequencies of damping. The frequency of a '1' is RF/10 and a '0' divides RF/8.

PSK Modulation

The coil is damped with a carrier frequency of RF/2. The data '1' causes a 180° phase shift on the carrier, while a '0' does no phase shift.

Manchester Modulation

Logical '1' makes a falling edge during a bit time (i.e., switch damping on). The '0' makes a rising edge (i.e., switch damping off).

Biphase Modulation

The coil is damped with a carrier frequency which is similar to the bitclock at a '1'. A '0' doubles the carrier period.

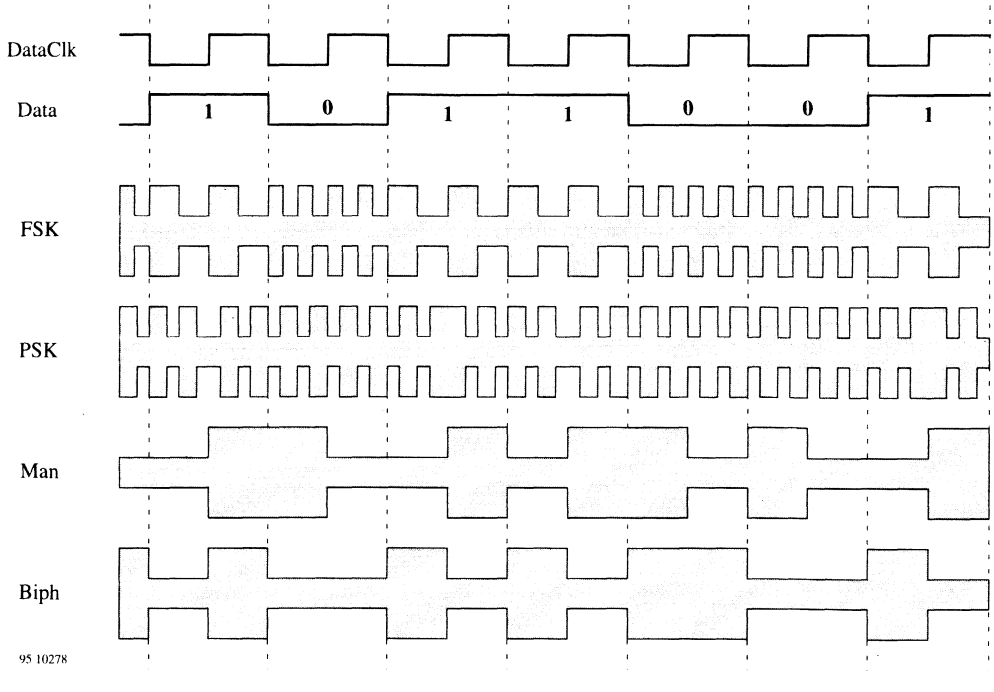


Figure 2. Types of modulation (shown as transponder coil voltage)

Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device.

Parameters		Symbol	Min.	Typ.	Max.	Unit
Operating ambient temperature		T_{op}	–40		85	°C
Storage temperature		T_{st}	–40		100	°C
Assembly temperature	< 5 min	T_{assy}		170		°C
Assembly pressure	isostatic	p_{assy}		50		°C

Electrical and Magnetic Characteristics

T_{amb} = 25°C unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Resonance frequency		f_{res}	121.25	125	128.75	kHz
LC quality	V_{coil} < 0.5 V	Q	13	17	21	–
Resonance frequency deviation	T = –40 to +85°C	Df_{res}	–1		+1	%
Coil inductance	L and C are ± 5%	L	3.99	4.20	4.41	mH
Resonance capacitor	(sorted to met f_{res+})	C	370	390	410	pF
Minimum magnetic field strength	@ f_{res}	H_{opmin}		6		A/m

Mechanical Characterristics

Parameters	Description	Comment	Value	Unit
Shock	6 shocks per axe, all 3 axes	IEC 68–2–27	1500	g
Vibration	100 to 20000 Hz, 6 h/ axe, 3 axes	IEC 68 2–27 Fc	5	g
Mechanical strength	Horizontal and vertical		5	N

Order Information

ID Code Selection

The customer can choose any ID code suitable to his application. To avoid code duplication, TEMIC will define a fixed header – i.e, the first 8 bits of the code – for each customer. For programming the code into the laser ROM, one of the following has to be supplied:

- ID code on floppy disk or per email (i.e., the customer is generating the codes). The format is:
  - ASCII format
  - Each line contain one ID code in hex notation
  - First 8 code bits must be the TEMIC-defined header
  - Each line must start with a unique sequence number (please refer to our "e5530 Code Format Application Note" for further details)
- ID code algorithm which is implemented in our code management software (i.e., we are generating the codes as necessary)

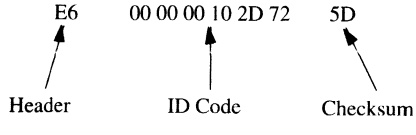


Figure 3. Example for a 64 bit code

Options

Further, the customer has to select the following operation options:

- Bitrate, which is defined as field clocks per bit (e.g., RF/40 = 125 kHz/40 = 3.125 kBit/s)
- Modulation (see page 2)
- Code length: 32, 64, 96 and 128 bits

Order Code

The full order code for the e5530GT transponder is **e5530H–xxx GT**, where xxx is the header number defined by TEMIC.

Application

Samples

TEMIC supplies e5530GT samples, which are set to Manchester modulation at RF/40 with a 64 bit ID code (order code: e5530H-230 GT).

Reader

To read the e5530GT transponder, a reader unit is necessary. Such a reader has to supply a sufficient magnetic field. Further, it must detect and decode the damping of the transponder in order to read the ID code.

TEMIC offers the U2270B, which implements all important analog functions for such a reader unit.

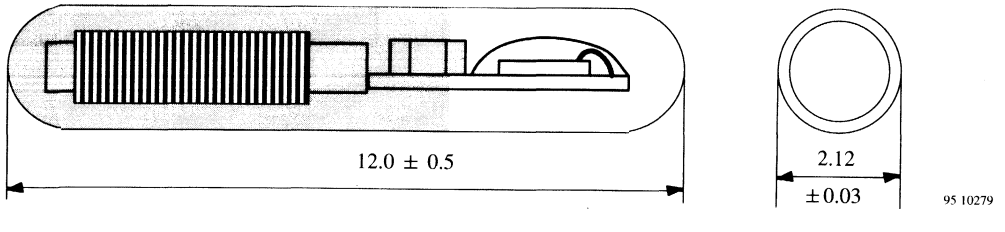
- Special coil driver for 5 V or 12 V
- Demodulator, input filter and amplifier to read Manchester or biphase transponder
- Microcontroller-compatible data output

Reading Distances

The e5530GT is able to operate from very weak fields. Nevertheless, there are some general rules which influence the achievable reading distance.

- Best results are accomplished when the transponder points towards the reader coil.
- The transponder should not be embedded in metal, which will reduce the applicable magnetic field and thus the reading distance.
- The strength of the generated magnetic field and the sensitivity of the demodulator are the most important factors for a good reading distance.
  (A typical system with a small coil and a simple demodulator may reach ~3 cm, whereas a fully optimized system may reach up to 20 cm.)

Dimensions in mm



e5550

Standard R/W Identification IC

Description

The e5550 is a contactless R/W-**ID**entification **IC** (IDIC®) for general-purpose applications in the 125 kHz range. A single coil, connected to the chip, serves as the IC's power supply and bidirectional communication interface. Coil and chip together form a transponder.

The on-chip 264 bit EEPROM (8 blocks 33 bits each) can be read and written blockwise from a reader unit. The blocks can be protected against overwriting. One block is reserved for setting the operation modes of the IC. Another block can contain a password to prevent un-authorized writing.

Reading occurs by damping the coil by an internal load. There are different bitrates and encoding schemes possible. Writing occurs by interrupting the RF field in a special way.

Features

- Low power, low voltage CMOS IDIC®
- Contactless power supply
- Contactless read/ write data transmission
- **R**adio **F**requency (RF): 100 to 150 kHz
- 264 bit EEPROM memory in 8 blocks of 33 bits
- 224 bits in 7 blocks of 32 bits are free for user data
- Block write protection
- Extensive protection against contactless malprogramming of the EEPROM
- Typical < 50 ms to write and verify a block
- Other options set by EEPROM:

Bitrate [bit/s]:	RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100, RF/128
Modulation:	BIN, FSK, PSK, Manchester, Biphase
Other:	Answer-On-Request (AOR), Terminator mode, Password mode

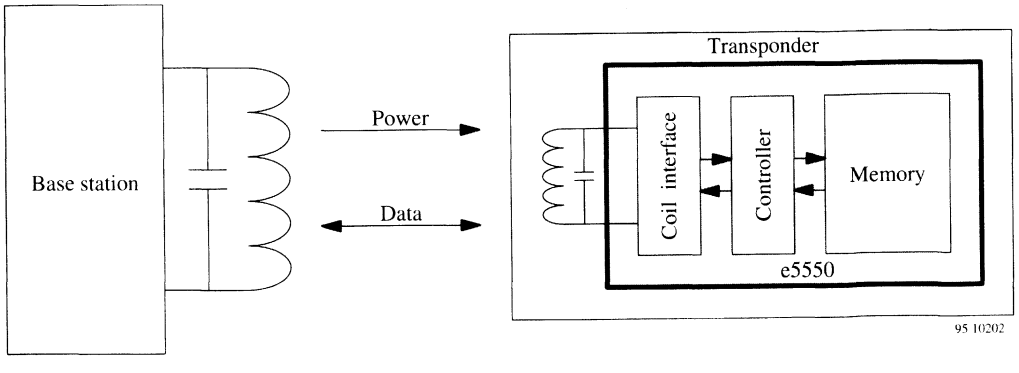
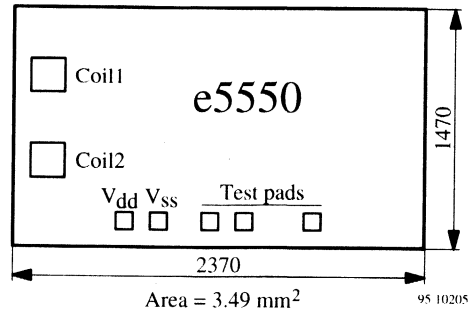


Figure 1.

Pads

Pads	Pad Windows	Function
Coil1	136 × 136 µm²	1st coil pad
Coil2	136 × 136 µm²	2nd coil pad
V_{dd}	78 × 78 µm²	Positive supply voltage
V_{ss}	7 × 78 µm²	Negative supply voltage (gnd)
Test1	78 × 78 µm²	Test pad
Test2	78 × 78 µm²	Test pad
Test3	78 × 78 µm²	Test pad

Chip Dimensions



e5550 Building Blocks

Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil. It generates the IC's power supply and handles the bidirectional data communication with the reader unit. It consists of the following blocks:

- Rectifier to generate a dc supply voltage from the ac coil voltage
- Clock extractor
- Switchable load between Coil1/ Coil2 for data transmission from the IC to the reader unit (read)
- Field gap detector for data transmission from the reader unit into the IC (write)

Controller

The main controller has following functions:

- Load mode register with mode data from EEPROM block 0 after power-on and also during reading
- Control memory access (read, write)
- Handle write data transmission and the write error modes
- The first two bits of the write data stream are the header bits. There are two valid headers (standard and stop) which are decoded by the controller.
- In password mode, the 32 bits received after the header are compared with the stored password in block 7.

Bitrate Generator

The bitrate generator can deliver the following bitrates:
rf/8 – rf/16 – rf/32 – rf/40 – rf/50 – rf/64 – rf/100 – rf/128

Write Decoder

Decode the detected gaps during writing. Check if write data stream is valid.

Test Logic

Test circuitry allows rapid programming and verification of the IC during test.

HV Generator

Voltage pump which generates ~18 V for programming of the EEPROM.

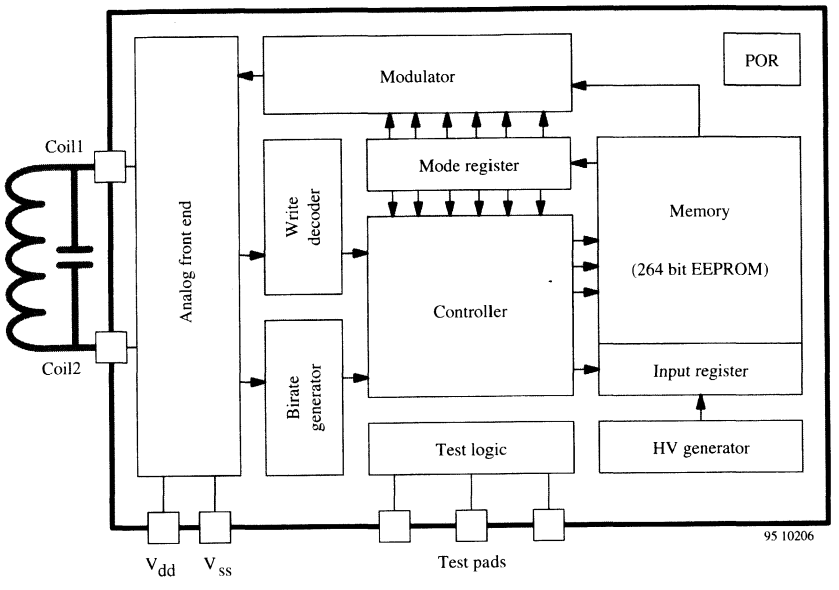


Figure 2. Block diagram e5550

Power-On Reset (POR)

The power-on reset is a delay reset which is triggered when supply voltage is applied.

Mode Register

The mode register stores the mode data from EEPROM block 0. It is continually refreshed at the start of every block. This increases the reliability of the device (if the originally loaded mode information is false, it will be corrected by subsequent refresh cycles).

Modulator

The modulator consists of several data encoders in two stages, which may be freely combined to obtain the desired modulation. The basic types of modulation are:

- PSK: phase shift: 1) every change; 2) every '1'; 3) every rising edge (carrier: fc/2, fc/4 or fc/8)
- FSK: 1) f1 = rf/8 f2 = rf/5; 2) f1 = rf/8 f1 = rf/10
- Manchester: rising edge = H; falling edge = L
- Biphase: every bit creates a change, a data 'H' creates an additional mid-bit change

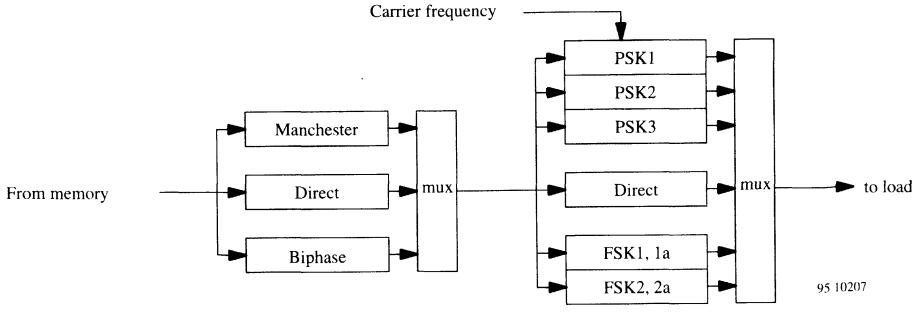


Figure 3. Modulator block diagram

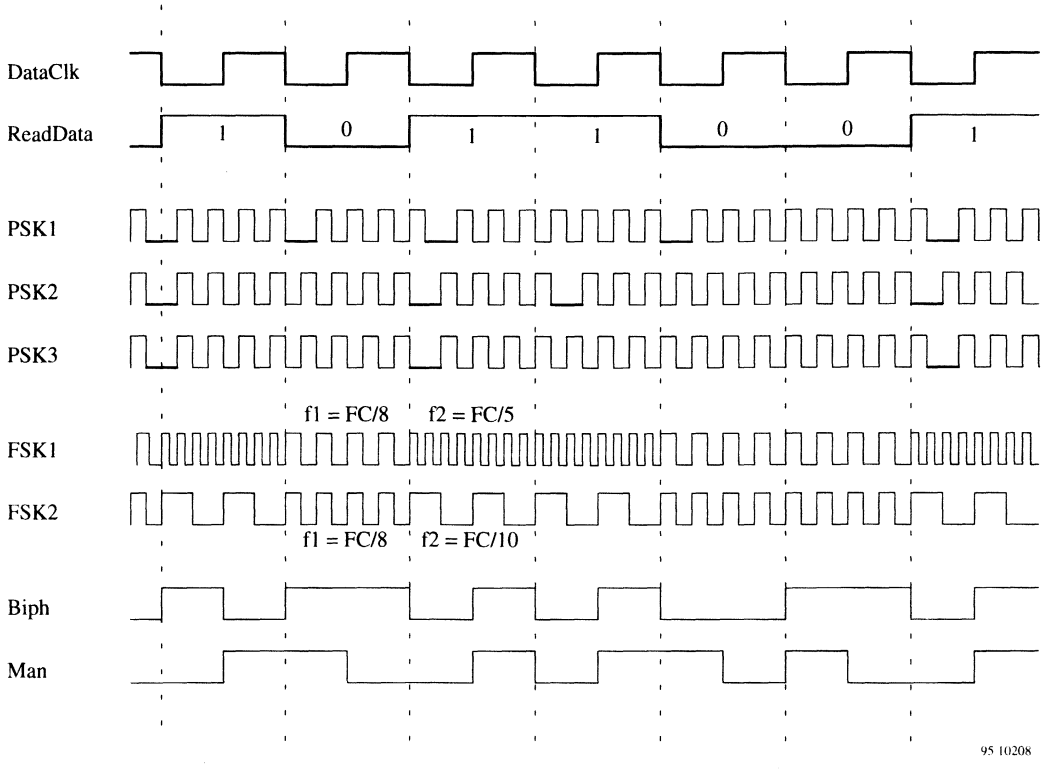


Figure 4. Types of modulation

Note: The following modulation type combinations will not work:

- Stage1 Manchester or Biphase, stage2 psk2, at any psk carrier frequency (because the first stage output frequency is higher than the second stage strobe frequency)
- Stage1 Manchester or Biphase and stage2 psk with bitrate = rf/8 and psk carrier frequency = rf/8 (for the same reason as above)
- Any stage1 option with any psk for bitrates rf/50 or rf/100 if the psk carrier frequency is not an integer multiple of the bitrate (e.g., br = rf/50, pskcf = rf/4, because 50/4 = 12.5). This is because the psk carrier frequency must maintain constant phase with respect to the bit clock.

Memory

The memory of the e5550 is a 264 bit EEPROM, which is arranged in 8 blocks of 33 bits each. All 33 bits of a block, including the lock bit, are programmed simultaneously. The programming voltage is generated on-chip.

Block 0 is reserved for mode data; it is not normally transmitted (see figure 6).

Block 1 to 6 are freely programmable. Block 7 may be used as a password. If password protection is not required, it may be used for user data.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lockbit itself) cannot be field-reprogrammed. It is only possible to override a write-protect bit in test mode; this requires access to the WTEST, RTEST and PRST pads.

Data from the memory is transmitted serially, starting with block 1, bit 1, up to block 'maxblk', bit 32. 'Maxblk' is a mode parameter set by the user to a value between 0 and 7 (if maxblk=0, only block 0 will be transmitted).

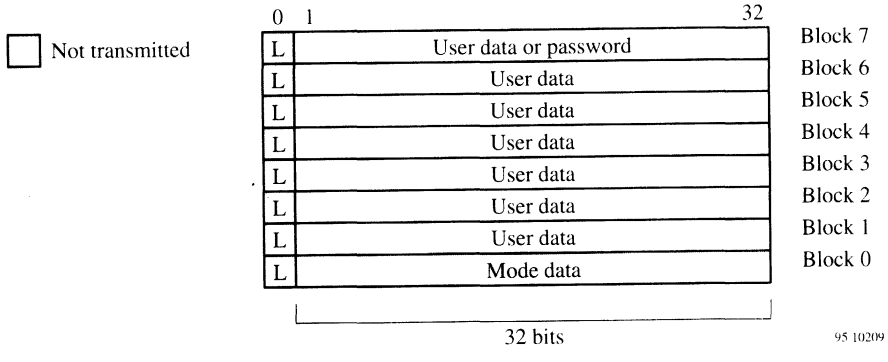


Figure 5. Memory map

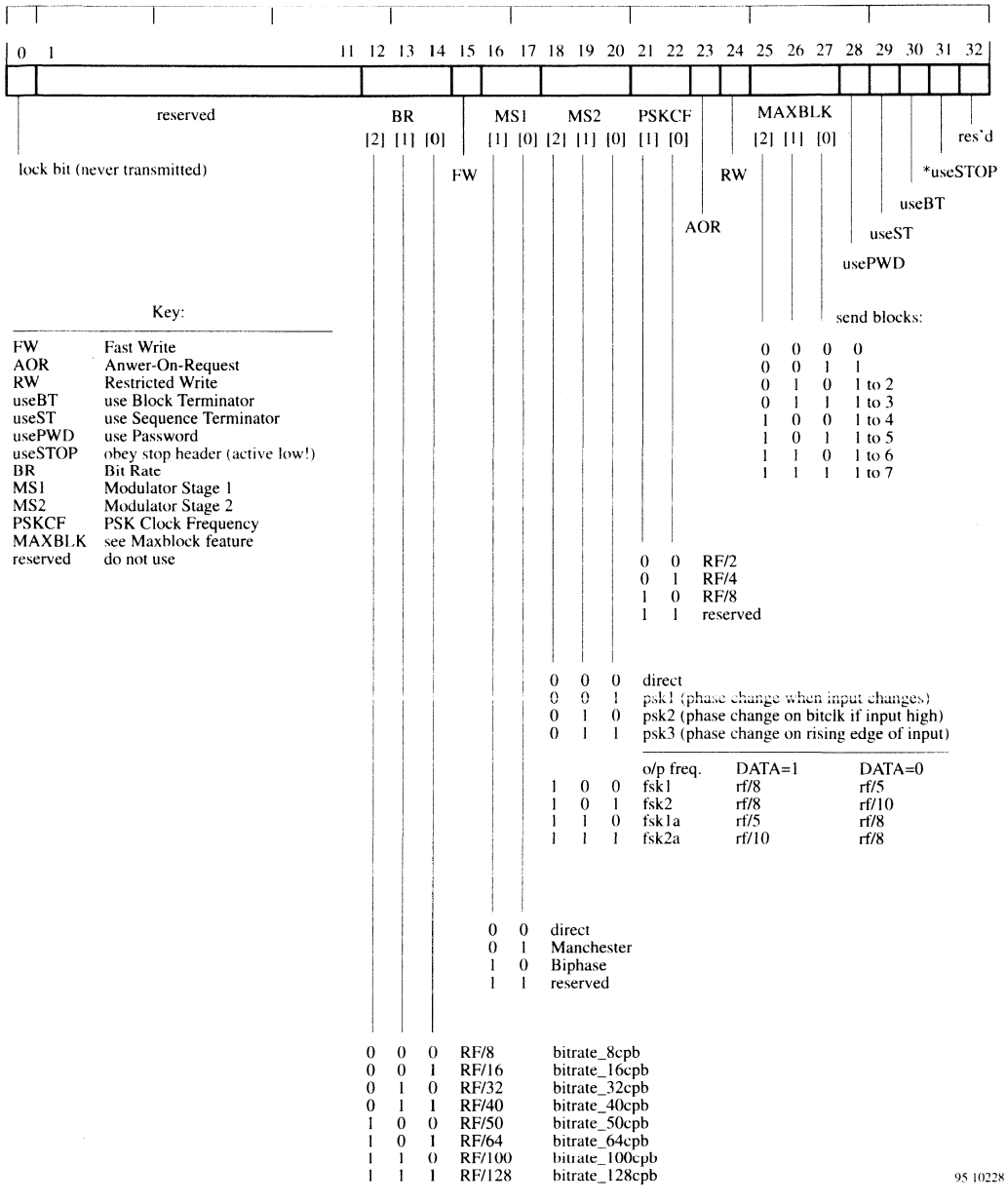


Figure 6. Memory map of block 0

Operating the e5550

General

The basic functions of the e5550 are: **supply** IC from the coil, **read** data from the EEPROM to the reader, **write** data into the IC and **program** these data into the EEPROM. Several **errors** can be detected to protect the memory from being written with the wrong data (see figure 20).

Supply

The e5550 is supplied via a tuned LC circuit which is connected to the Coil1 and Coil2 pads. The incoming RF (actually a magnetic field) induces a current into the coil which powers the chip. The on-chip rectifier generates the dc supply voltage (V_{dd}, V_{ss} pads). Overvoltage protection prevents the IC from damage due to high-field strengths. (Depending on the coil, the open-circuit voltage across the LC circuit can reach more than 100 V). The first occurrence of RF triggers a power-on reset pulse, ensuring a defined start-up state.

Read

Reading is the default mode after power-on reset. It is done by switching a load between the coil pads on and off. This changes the current through the IC coil, which can be detected from the reader unit.

Start-Up

The many different modes of the e5550 are activated after the first readout of block 0. The modulation is off while block 0 is read. After this set-up time of 256 field clock periods, modulation with the selected mode starts.

Read Datastream

The first block transmitted is block 1. When the last block is reached, reading restarts with block 1. Block 0, which contains mode data, is normally never transmitted. However, the mode register is continuously refreshed with the contents of EEPROM block 0.

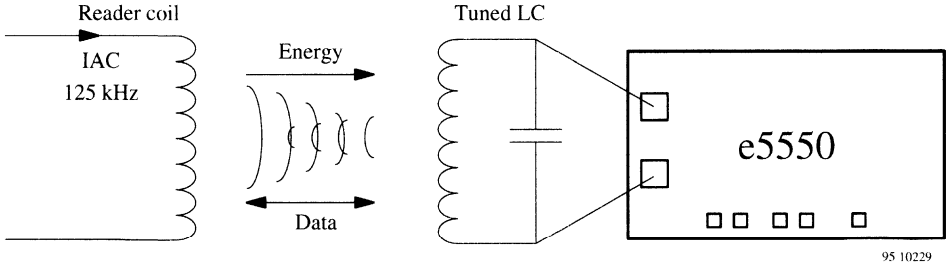


Figure 7. Application circuit

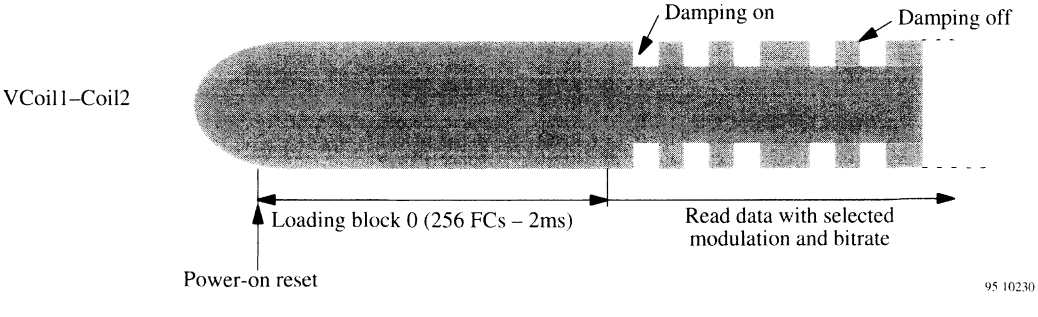


Figure 8. Voltage at Coil1/Coil2 after power-on

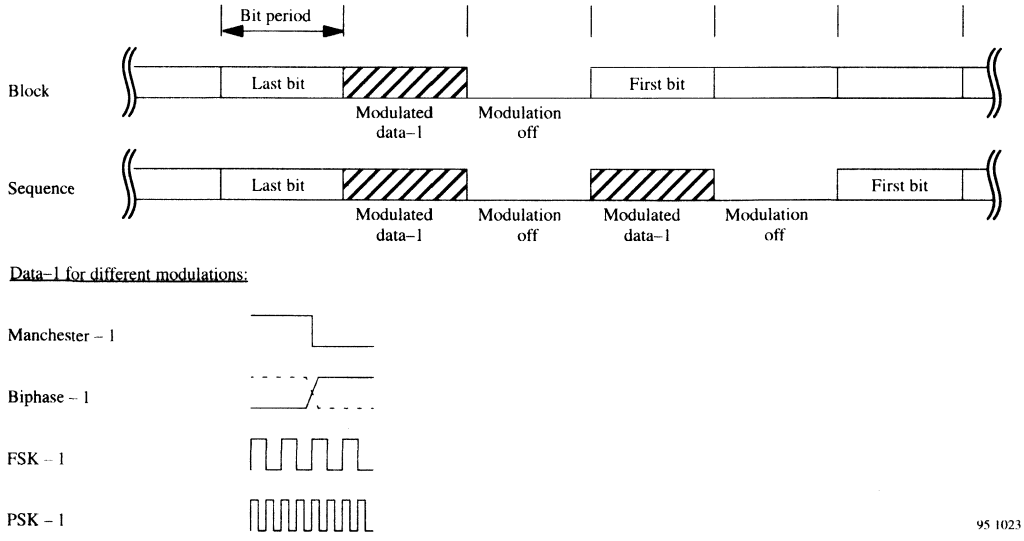


Figure 9. Terminators

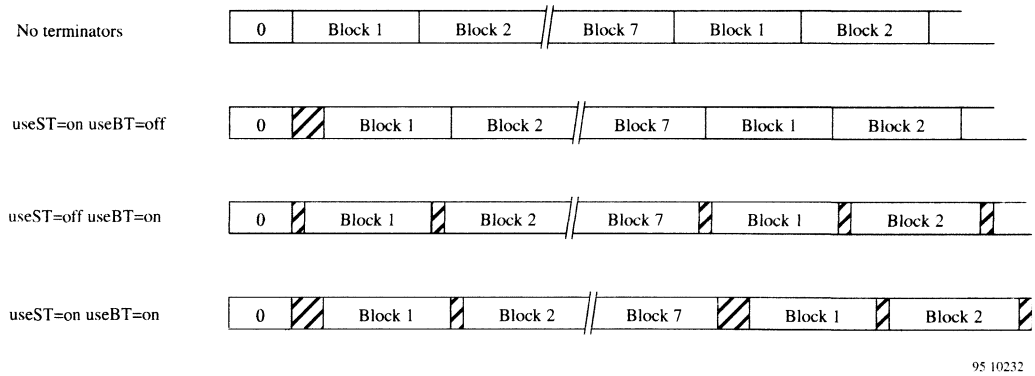


Figure 10. Read data streams and terminators

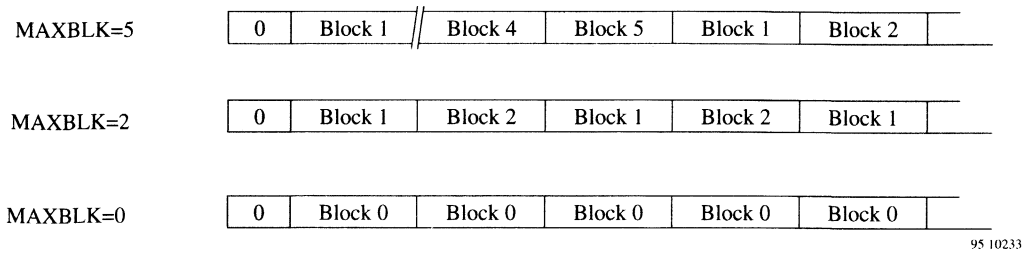


Figure 11. MAXBLK examples

Terminators

The terminators are (optionally selectable) special damping patterns, which may be used to synchronize the reader. There are two types available; a block terminator which precedes every block, and a sequence terminator which always follows the last block.

The sequence terminator consists of two consecutive block terminators. The terminators may be individually enabled with the mode bits useST (sequence terminator enable) or use BT (block terminator enable).

Note: The combination useST = 1 and useBT = 0 with MAXBLK = 0 causes the e5550 to transmit a continuous stream of terminators. It is not possible to include a sequence terminator in a transmission where MAXBLK = 0.

Modulation and Bitrate

There are two modulators in the e5550 (see figure 3) whose mode can be selected using the appropriate bits in block 0 (MS1[1:0] and MS[2:0]). Also the bitrate can be selected using BR[2:0] in block 0. These options are described in detail in figure 6.

Maxblock Feature

If it is not necessary to read all six user data blocks; the MAXBLK field in block 0 can be used to limit the number of blocks read. For example, if MAXBLK = 4, the e5550 repeatedly reads and transmits only blocks 1 to 4. If MAXBLK is set to '0', block 0 (which is normally hidden) is read.

Answer-On-Request (AOR) Mode

When the AOR bit is set, the IC does **not** start modulation after reading block 0. It waits for a valid signal from the reader before modulation is enabled. This is used for applications where 'tag is here' information is supplied by some additional means (e.g., turning the key which contains a tag). Therefore, in AOR mode, it is not possible to read the tag by simply applying an RF field. The activation pattern (request), which re-enables modulation, is a standard header followed by a valid password. If the usePWD bit is not set, any 32 valid bits will do in place of the password. The IC will remain active until the power is cycled, or a stop header is sent if useSTOP is active (low).

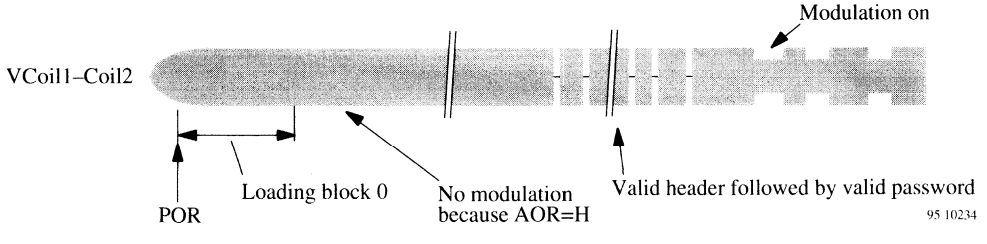


Figure 12. Answer-on-request mode

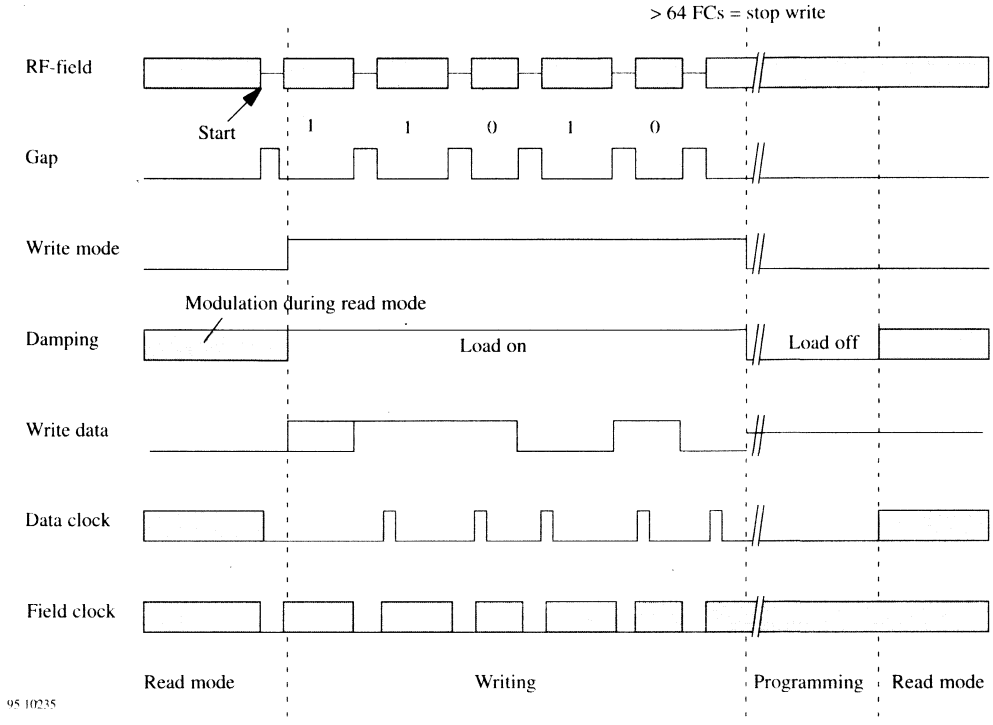


Figure 13. Signals during writing

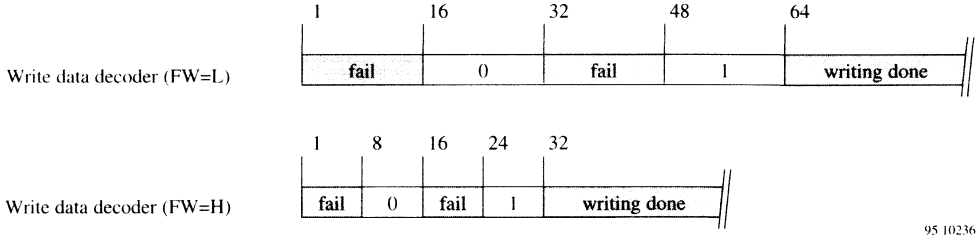


Figure 14. Write data decoding schemes

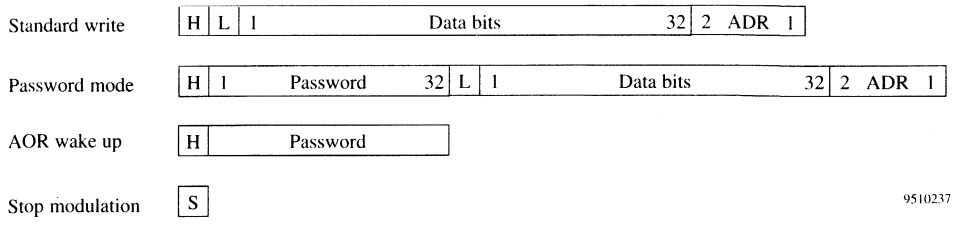


Figure 15. Legal write data sequences

Write

Writing data into the IC occurs via the TEMIC/Eurosil write method (patent pending). It is based on interrupting the RF field with short gaps. The time between two gaps encodes the '0/1' information to be transmitted.

Start Gap

The first gap is the start gap which triggers write mode. In write mode, the damping is permanently enabled which eases gap detection. The start gap may need to be longer than subsequent gaps in order to be detected reliably.

By default, a start gap will be detected at any time after block 0 has been read (field-on plus approximately 2 ms). When the restricted write mode bit (RW) is set, a start gap is only recognized during a terminator (block or sequence). When no terminator is active, the RW bit has no effect.

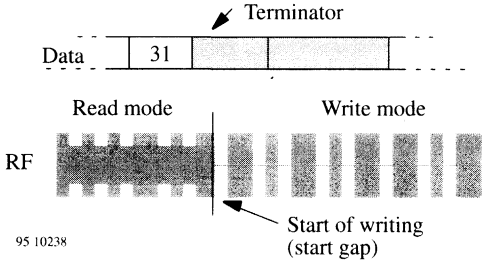


Figure 16. Start of writing in restricted write mode

Decoder

The duration of the gaps is usually 50 to 150 µs. The time between two gaps is nominally 24 field clocks for a '0' and 56 field clocks for a '1'. When the fast write mode bit (FW) is set, the decoding scheme is changed to enable faster (× 2) write data transmission. When there is no gap for more than 64 (or 32) field clocks after previous gap, the IC exits write mode; it starts with programming if the correct number of valid bits were received.

If there is a gap fail – i.e., one or more of the gaps was not a valid '0' or '1' – the IC does not program, but enters read mode beginning with block 1.

Writing Data into the e5550

The e5550 expects always to receive a header first. This header may be followed by different information:

- Standard writing needs only the header, the block address, the lock bit and the 32 data bits.
- Writing with usePWD set requires a valid password between header and address/data bits.
- In AOR mode, header and a valid password are necessary to enable modulation.
- A special header which is used to silence the e5550 (disable damping until power is cycled) is necessary.

Note: The data bits are read in the same order as written.

Headers

There are two valid headers. If the header is invalid, the e5550 starts read mode beginning with block 1 after the last gap.

The standard header ('10') precedes all write operations. The stop header ('11') is used to stop the IC until a power-on reset occurs. This feature can be used to have a steady RF field where single transponders are collected one by one. Each IC is read and than disabled, so that it does not interfere with the next IC.

Note: The stop header should contain only the two header bits to disable the IC. Any additional data sent will not be ignored, and the IC will not stop modulation.

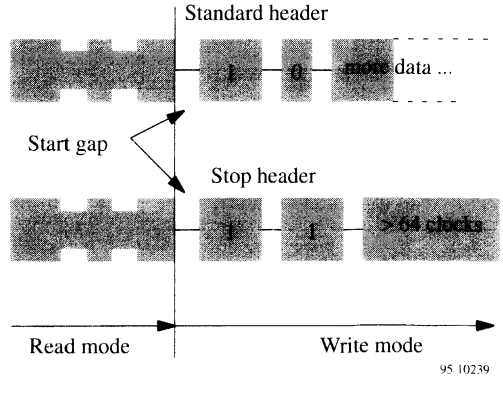


Figure 17. Headers

Password

When password mode is on (usePWD = 1), the first 32 bits after the header are regarded as the password. They are compared bit-by-bit with the contents of block 7, starting at bit 1. If the comparison fails, the IC will not program the memory, but restart in read mode at block 1 once writing has completed.

Note: If usePWD is not set, but the IC receives a write datastream containing any 32 bits in place of a password, the IC will enter programming mode.

Note: In password mode, MAXBLK should be set to a value below 7 to prevent the password from being transmitted by the e5550.

Note: Every transmission of 2 header bits plus 32 bits password plus 3 bits address plus 33 bits data (= 69 bits) needs about 35 ms. Testing all 2^{32} possible combinations (about 4.3 billion) takes about 40,000 h, or over four years. This is a sufficient password protection for a general-purpose IDIC.

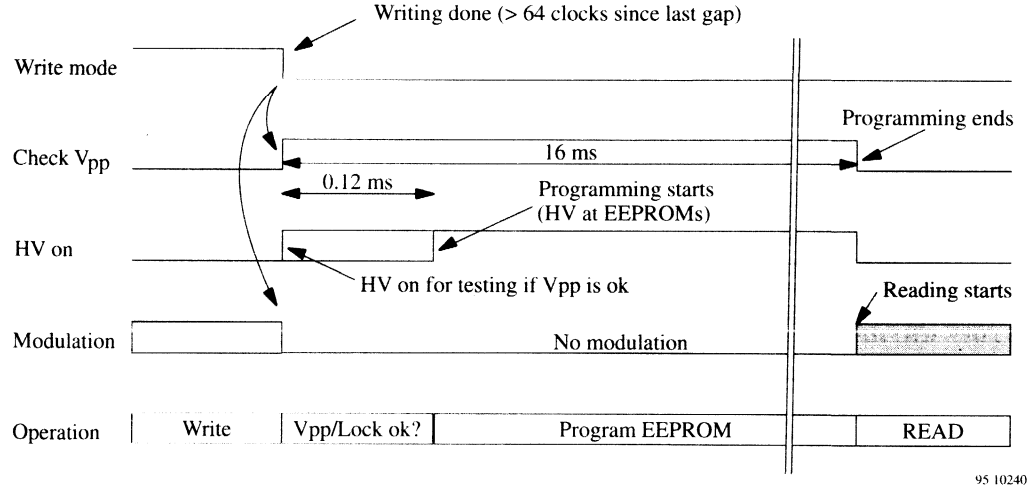


Figure 18. Programming

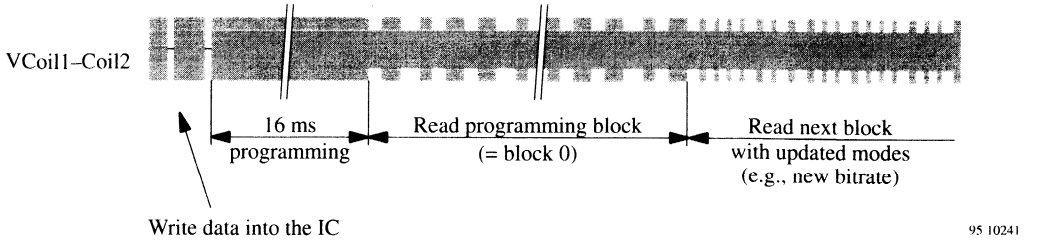


Figure 19. Coil voltage after programming

Programming

When all necessary information has been written to the e5550, programming may proceed. There is a 32-clock delay between the end of writing and the start of programming. During this time, Vpp – the EEPROM programming voltage – is measured and the lock bit for the block to be programmed is examined. Further, Vpp is continually monitored throughout the programming cycle. If at any time Vpp is too low, the chip enters read mode immediately.

The programming time is 16 ms.

After programming is done, the e5550 enters read mode, starting with the block just programmed. If either block or sequence terminators are enabled, the block is preceded by a block terminator. If the mode register (block 0) has been reprogrammed, the new mode will be activated **after** the just-programmed block has been transmitted using the **old** mode.

Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the EEPROM. There are two error types, which lead to two different actions.

Errors during writing

There are four detectable errors which could occur during writing data into the e5550:

- Wrong number of field clocks between two gaps
- The header is neither the standard header nor the stop header
- Password mode is active but the password does not match the contents of block 7
- The number of bits received is incorrect; valid bit counts are
  - Standard write 38 bits (usePWD not set)
  - Password write 70 bits (usePWD set)
  - AOR request 34 bits
  - Stop command 2 bits

If any of these four conditions are detected, the IC starts read mode immediately after leaving write mode. Reading starts with block 1.

Errors During Programming

If writing was successful, the following errors could prevent programming:

- The lock bit of the addressed block is set
- V_{PP} is too low

In these cases, programming stops immediately. The IC reverts to read mode, starting with the currently-addressed block.

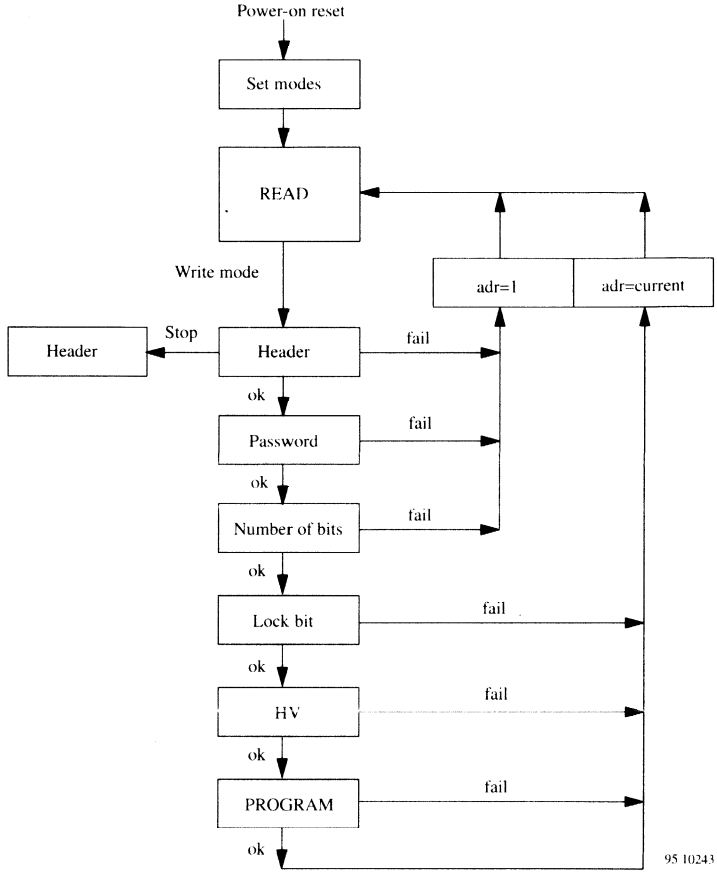


Figure 20. Functional diagram of the e5550

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage ($V_{dd} - V_{ss}$)		–0.3 to +7	V
Input voltage range		(V_{ss} – 0.3 V) to (V_{dd} + 0.3 V)	
Maximum current into COIL1/COIL2		10	mA
Power dissipation (dice) [1]		100	mW
Operationg ambient temperature range		–20 to +70	°C
Storage temperature range [2]		–40 to +125	°C
Maximum assembly temperature		+150°C for less than 5 min	

Notes: 1) Free-air condition, time of application: 1 s
2) Data retention reduced
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Operating Characteristics

$T_{ambient}$ = 25°C; reference terminal is V_{ss}, operating voltage $V_{dd} - V_{ss}$ = 3 V dc (unless otherwise noted)

Parameters	Comments	Symbol	Min.	Typ.	Max.	Unit
RF frequency range		f_{RF}	100	125	150	kHz
Supply current	f_{RF} = 125 kHz, Read and write	I_{dd}		5		µA
	Programming			250		µA
Clamp voltage	5 mA current into Coil1/2	V_{cl}	6		8	V
Programming voltage	From on-chip HV Gen	V_{pp}	16		20	V
Programming time	f_{RF} = 125 kHz	t_{PP}		16		ms
Data retention	1)	$t_{retention}$	10			Years
Programming cycles	1)	n_{cycle}	100 000			
Reset delay time		t1	0		tbd.	µs
Reset recovery time		t2	tbd.	tbd.	tbd.	ms

Note
1) Since EEPROM performance may be influenced by assembly and packaging, we can confirm the parameters for dow (= die-on-wafer) and ICs assembled in standard package.

Application Example

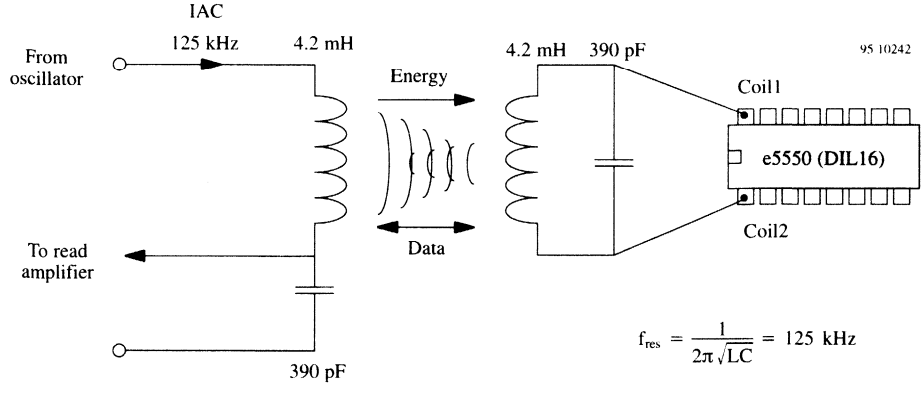


Figure 21. Typical application circuit

Crypto IDIC® for Transponder

General Description

Contactless **ID**entification **IC**s (IDICs®) are used to build transponder, which are small, smart and robust data storage units. The IDIC® is connected to a tuned LC circuit for power supply and R/W data communication between a base station and the IDIC®.

Reading occurs by damping the coil by an internal load. There are different bitrates and encoding schemes possible. Writing occurs by interrupting the RF field in a special way.

The e5560 is for applications which demand higher security levels as standard R/W transponder ICs can fullfil.

For that purpose, the e5560 has an encryption algorithm block which enables a base station to authenticate the transponder. Any attempt to fake the base station with a wrong transponder will be recognized immediately. Furthermore, the e5560 is able to do an authentication of the base station, to control the access to its memory.

Authentication Procedures

For authentication, the base station transmits a random number to the e5560. This challenge is encrypted by both, IC and base station. As both should posses the same secret key, the results of this encryption are expected to be equal.

To authenticate the transponder, the IC's results are transmitted to the base station for comparison (response). The e5560 can also check a response from the base station for authentication.

Features

- Low power, low voltage CMOS IDIC®
- Contactless power supply
- Contactless read/ write data transmission
  - Read: damping load (typ: 1 to 16 kbit/s)
  - Write: field gaps (typ: ~2 kbit/s)
- **R**adio **F**requency (RF) range: 100 to 150 kHz
- 1024 bit EEPROM memory
  - 768 bits free for user data (= 96 byte)
  - 256 bits for encryption (also for user data)
  - lockable memory blocks
- On-chip crypt algorithm for authentication
- Encryption time < 100 ms
- Options set by EEPROM:
  - Bitrate [bit/s]: RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100, RF/128
  - Modulation: BIN, FSK, PSK, Manchester, Biphase
  - Other: Answer_on_Request, Password_Mode
- Packaging
  - Bare die
  - Plastic transponder (12 × 6 × 3 mm^3)
- Applications:
  - Access control
  - Car immobilizer
  - Identification of valuable goods
  - Applications with high memory demand

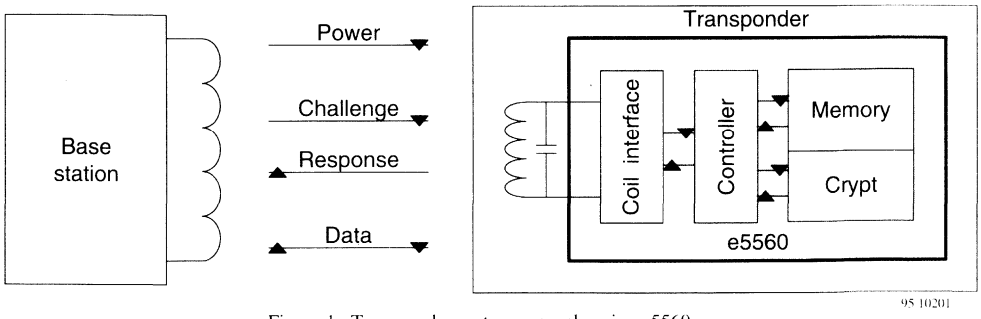


Figure 1. Transponder system example using e5560

General Information

Keyless Entry

Immobilizer

Microcontroller

Addresses

MARC4 – 4-bit Microcontroller

The M43C200 is a member of the TEMIC family of 4-bit single chip microcontroller. It contains ROM, RAM, parallel I/O ports and on-chip clock generation.

Features

- **Stack oriented HARVARD architecture**
  - 4K × 8-bit ROM
  - 256 × 4-bit RAM
  - 2 µs instruction cycle @ 4 MHz OSC-frequency
- **Programming**
  - User friendly in high level language qForth
- **Development system**
  - PC-based
  - Highly optimising compiler
- **Low power**
  - STOP mode @ 1 µA
  - SLEEP mode typically 500 µA
  - RUN mode typically 3 mA
- **High operating range**
  - Supply voltage range 2.4 to 6.2 V
  - Temperature range –40 to 85°C
- **Interrupt structure**
  - 2 external hardware interrupts
  - 1 prescaler/timer interrupt
  - Software interrupts
  - Autosleep

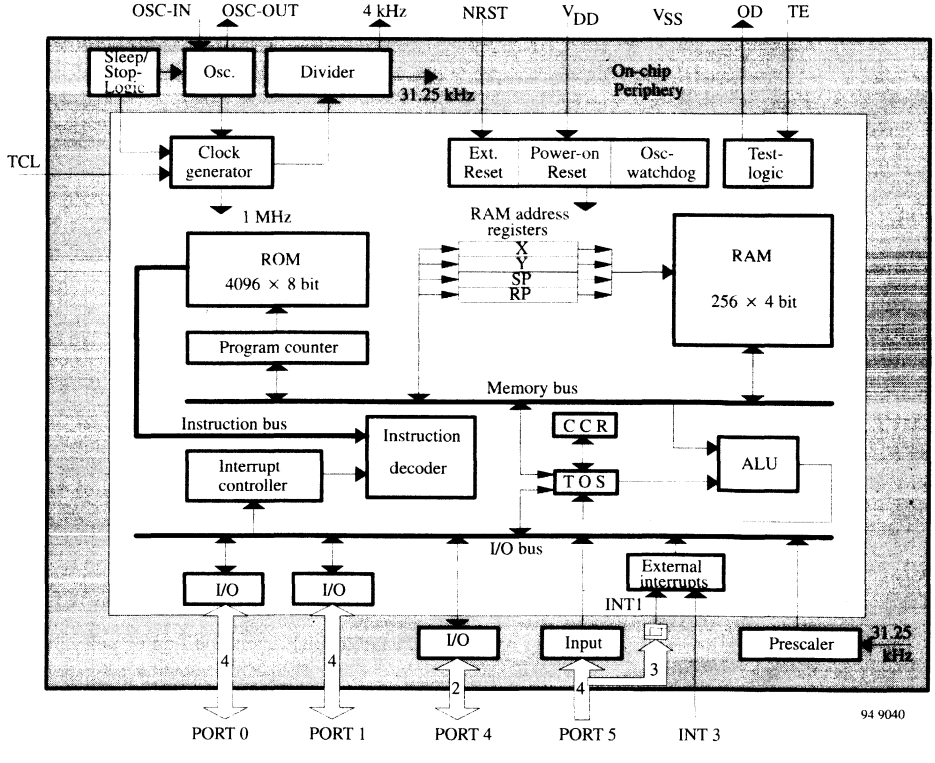


Figure 1. Functional block diagram

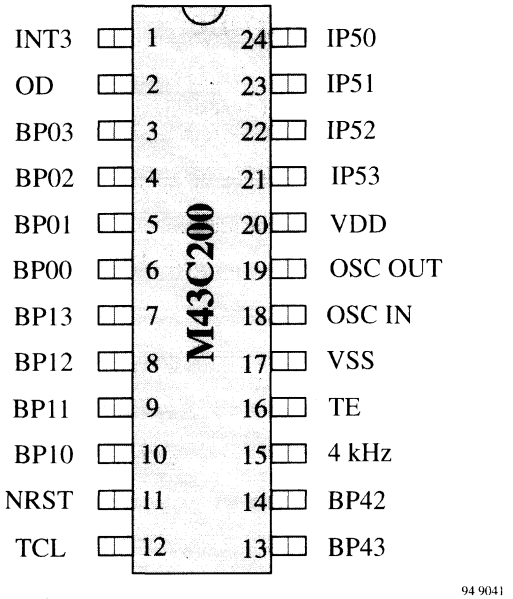


Figure 2. Pin assignment SO24 (top view)

Table 1. Pin description

Pin	Function
V_{DD}	Power supply voltage 2.4 to 6.2 V
V_{SS}	Circuit ground
BP00 – BP03	4 bidirectional I/O lines of port 0 *)
BP10 – BP13	4 bidirectional I/O lines of port 1 *)
BP42 – BP43	2 bidirectional I/O lines of port 4 *)
IP50 – IP53	4 input lines of port 5
OSCIN	Oscillator input (32-kHz crystal)
OSCOUT	Oscillator output (32-kHz crystal)
INT3	External interrupt input
4 kHz	4 kHz output
OD	OD signal for emulation
NRST	Reset input / output, a logic low on this pin resets the device.
TCL	External system clock I/O. This pin can be used for external clock operation.
TE	Testmode input. This input is used to control the test modes and the function of the TCL pin.

*) The I/O ports have CMOS output buffers. As input they are available with pull-up or pull-down resistors. Please see the order information.

Table of Contents

Table of Contents (continued)

1 General Description

The M43C200 is a member of the TEMIC MARC4 family (single chip **M**odular **ARC**hitecture **4**-bit microcomputers). It contains ROM, RAM, I/O-ports, 15 stage prescaler, 4-MHz oscillator and two external interrupts.

Note: For the self-test program about 0.5 Kbyte of the 4 Kbyte ROM are required.

The CPU is built around a stack based Harvard type architecture, where the program memory (in ROM) and the data memory (in RAM) are physically separate and addressed independently.

The M43C200 has a typical instruction cycle time of 2 µs @ 4 MHz oscillator frequency.

The SLEEP instruction allows the CPU to be stopped by the program, thereby enabling reduction in current consumption. Once the CPU has entered SLEEP mode it can be revived into active state immediately, following the receipt of an interrupt. In SLEEP mode, the CPU is held in a defined state whereby all data are latched. In the SLEEP mode the 4-MHz oscillator and the prescaler/ timer are still running. It gives the opportunity to wake up the CPU in a defined time which is given by the prescaler.

The highest power saving mode is the STOP mode. In this case the CPU, oscillator and prescaler are all stopped controlled by the internal NRUN-signal. If an interrupt appears the 4-MHz oscillator will be started, controlled by the SLEEP/ STOP logic. When the oscillator has reached the exact frequency a reset is generated and the program will start the $RESET routine.

1.1 Interrupt Structure

The MARC4 can handle up to eight priority interrupts which can be generated from on-chip modules (prescaler), external sources (interrupt pads) or synchronously from the CPU itself (software interrupts).

An additional power-on reset interrupt is used for initialising the CPU. This reset signal can also be supplied from the RST pad. The purpose of the power-on reset is to start the oscillator and to put the CPU into a well defined condition after the operating voltage has been reached. The reset interrupt has the absolute highest priority having access to the CPU at all times. The processor will automatically enter SLEEP when the lowest priority task has been completed, so making maximum use of the power saving capabilities of the MARC4.

1.2 Prescaler

A programmable prescaler driven by 31.25 kHz offers 1 interrupt. Table 2 (page 116) illustrates the eligible interrupt frequencies. The prescaler powers up in the reset condition.

2 Pin-, Signal-, Memory-, Core Registers- and Self-Check Description

2.1 Pin Description

2.1.1 V_{DD}, V_{SS}

V_{DD} is the power for the µC core, RAM, ROM and the peripherals, V_{SS} is ground.

2.1.2 NRST

The NRST input is not required for start-up but can be used to reset state of the microcontroller and provide an orderly software start-up procedure. Refer to **Reset modes** in section for a detailed description.

2.1.3 TCL

The system clock for the microprocessor is derived from a fully integrated on-chip crystal oscillator circuit. This oscillator tracks the supply and temperature to ensure optimum operation of the microcontroller under all conditions.
The TCL pin is necessary as clock input for the test- and emulation mode.

2.1.4 TE, OD

These two lines are needed for test and emulation.

2.1.5 OSCIN, OSCOUT

An oscillator with a divider stage is integrated in the chip to generate the 1-MHz clock frequency (TCL). This oscillator is operated by simple connection of 4-MHz quartz or ceramic resonator.

This oscillator can be controlled via port 42 (NRUN-signal). This means that the oscillator can be stopped in SLEEP mode or remains active if operation of the prescaler is desired. However, this function can only be set by software.

INRUN – signal "high"
the µC goes in sleep mode after finishing the lowest (Port 42) interrupt (oscillator running)

INRUN – signal "low"
the µC goes in STOP mode after finishing the lowest interrupt (oscillator stop).

2.1.6 Bidirectional Ports

Port 0, 1 and 4 may be programmed as input or output under software control. The direction of a port is determined by an IN or OUT instruction and is held until another IN or OUT instruction for this port is executed.

The direction of this bidirectional ports is not switchable on a bit-wise basis. The output latches hold the state of last data value written to the port. At power-on or external reset all pins of port 0, 1 and 4 are set to input mode and all output latches are set to a logic 1. Whenever the port is switched from input to output the last value stored in the latches will appear on the outputs for one clock cycle.

When switching bidirectional ports from output to input the stray capacitance of the connection wires may cause the data read to be the same as the last data written to this port. This behaviour can be used by connecting large enough capacitors to the pins of the bidirectional port to read back the previous data written to this port. On the other hand, to avoid the negative effects of stray capacitance the following approaches should be used:
Use two IN instructions, and DROP the first data nibble read.

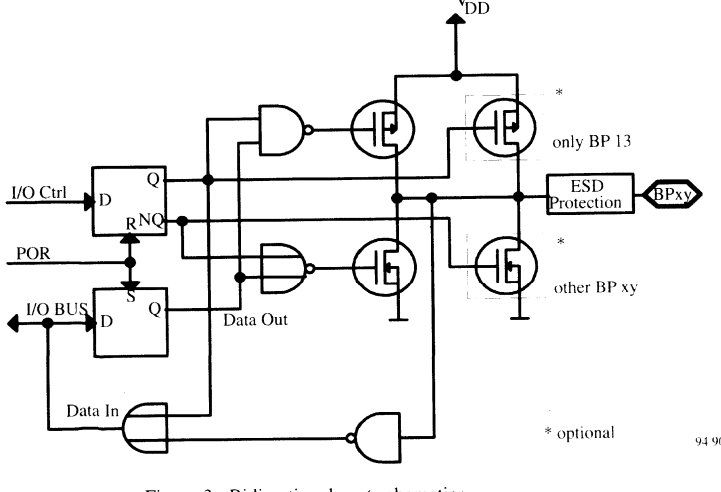
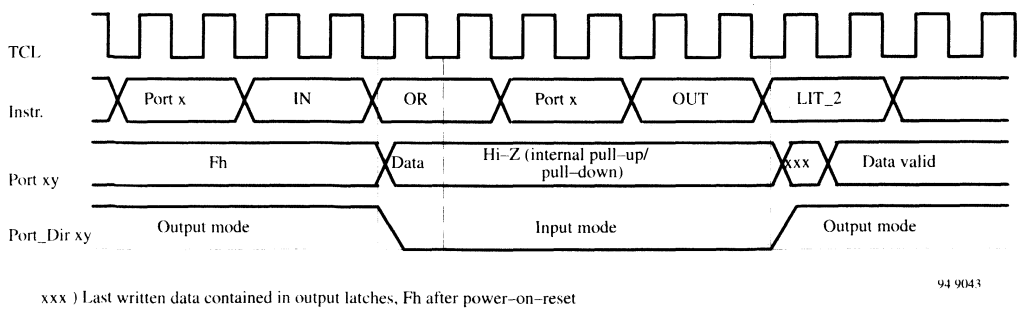


Figure 3. Bidirectional port schematics



xxx) Last written data contained in output latches, Fh after power-on-reset

Figure 4. Read and write cycle timing

2.1.7 Input Port 5

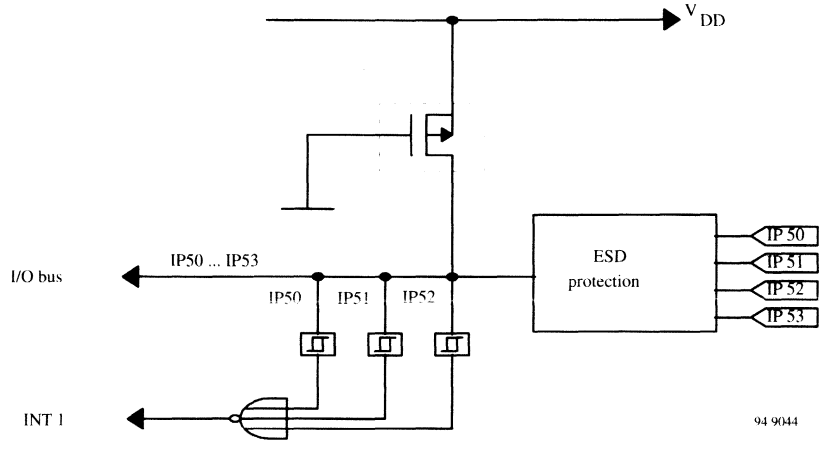


Figure 5. Input port

The data on port 5 is sent to the top of the expression stack whenever an IN instruction (addressing port 5) is executed. The pins IP50, IP51 and IP52 of the port 5 may generate an additional interrupt (priority level 1), when any of the three input lines is driven low. This function is useful for implementing an interrupt driven keyboard. The interrupt lines are negative edge triggered and have Schmitt-trigger characteristics to improve the noise immunity. The interrupt function is enabled after power-on or external reset. This interrupt can be disabled by software.

2.2 Memory

The MARC4 family of microcontroller is based on the Harvard architecture with physically separate program memory (ROM) and data memory (RAM).

The program memory (ROM) is mask programmed with the customer application program during the fabrication of the microcontroller. The ROM is addressed by a 12-bit wide program counter, thus limiting the program size to a maximum of 4096 bytes which cannot be extended by using external memory. The user ROM starts with a 512 byte segment ('Zero Page') which contains predefined start addresses for interrupt service routines and special subroutines accessible with single byte (SCALL) instructions. The corresponding memory map is shown in figure 6.

The self test routines should be included as part of the free program space. The 16-bit check sum (CRC) is located by the compiler in the last two bytes of ROM.

The on-chip 256 × 4 bit RAM is divided in the 12-bit wide return stack, the 4-bit wide expression stack (both with a user definable depth) and the data memory. The fixed return address (00h) which points to the $AUTO-SLEEP routine is located at RAM address FCh.

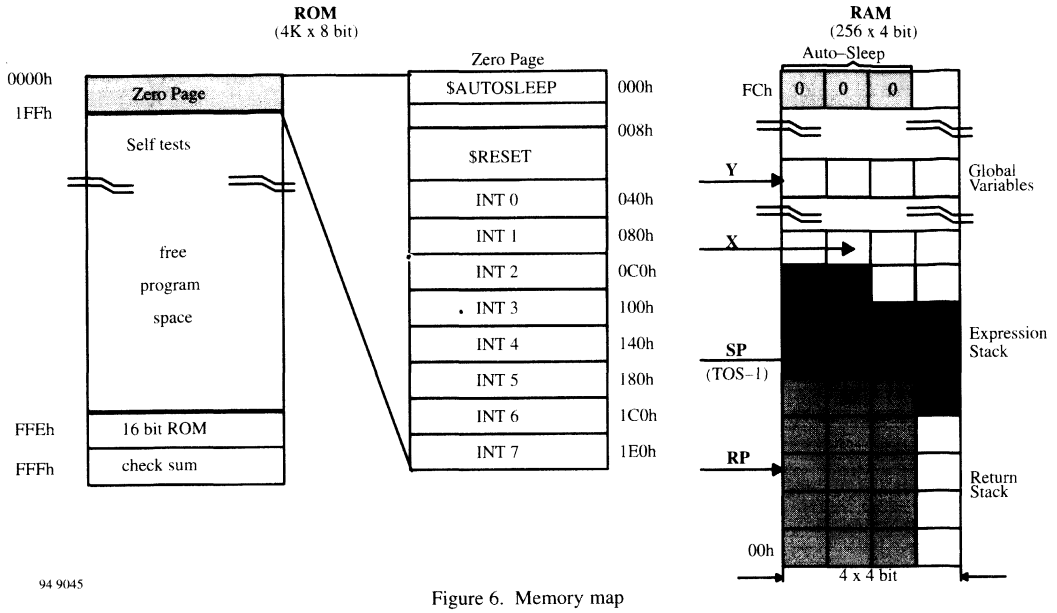


Figure 6. Memory map

2.3 Core Registers

As shown in the programming model below, the MARC4 core has seven registers.

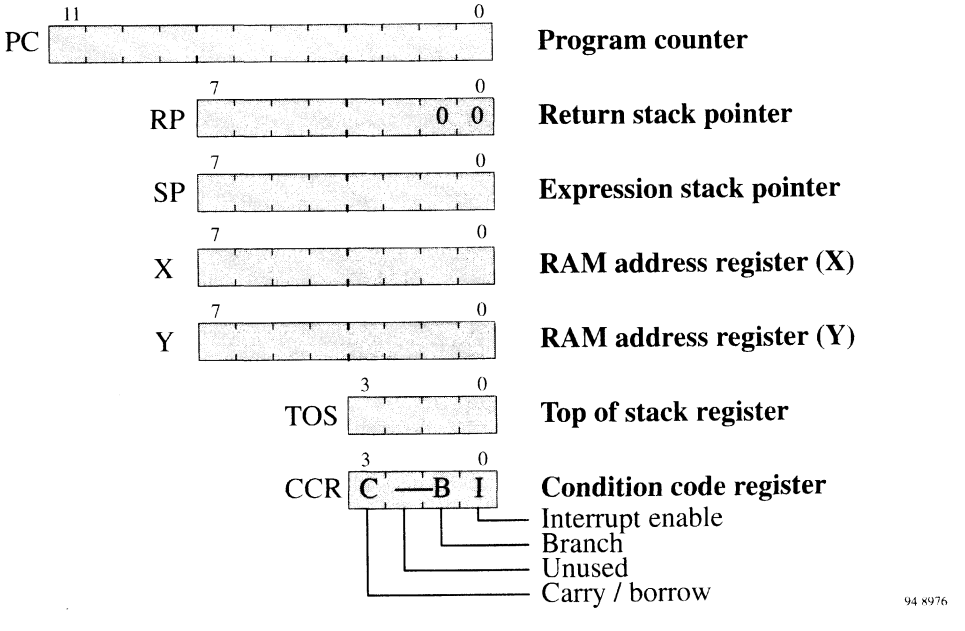


Figure 7. Programming model

2.3.1 Accumulator (TOS)

Because this microcontroller is a stack based machine with two on-chip stacks located in the internal RAM, all arithmetic, I/O and memory reference operations take their operands from, and return their results to the 4-bit wide expression stack. This stack is also used for passing parameters between subroutines, and as a scratchpad area for temporary storage of data. The top element of the expression stack is immediately accessible through the TOS register. The MARC4 can perform most of the operations dealing with the top of stack items (TOS and TOS-1) in a single byte, single cycle instruction.

2.3.2 Expression Stack Pointer (SP)

The 8-bit wide stack pointer SP contains the address of the next-to-top 4-bit item (TOS-1) on the expression stack, located in internal RAM. After power-on reset the stack pointer has to be initialised to the start address of the allocated expression stack area (S0).

2.3.3 RAM Address Register (X and Y)

The 8-bit wide register X and Y are used to address any 4-bit item in the RAM.

Using either the pre-increment address mode it is comfortable to compare, fill or move arrays in the RAM area.

2.3.4 Return Stack Pointer (RP)

The return stack pointer (RP) points to the top element of the return stack.

The 12-bit return stack is used for storing subroutine return addresses and keeping loop index counts. The return stack can also be used as a temporary storage area. The MARC4 instruction set supports the exchange of data between the top elements of the expression and return stack. The return stack automatically pre-increments and post-decrements in steps of 4. This means that every time a subroutine return address is stacked, 4-bit RAM locations are left unwritten. This locations are used by the qFORTH compiler to allocate 4-bit variables.

After power-on reset the return stack pointer has to be initialised to FCh.

2.3.5 Program Counter (PC)

The program counter (PC) is a 12-bit register that contains the address of the next instruction to be executed by the microcontroller.

2.3.6 Condition Code Register (CCR)

The 4-bit wide condition code register (CCR) indicates the results of instruction just executed as well as the state of the microcontroller. These bits can be individually tested by a program and specified action will take place as a result of their state. Each bit is explained in the following paragraphs.

Carry/Borrow (C)

This flag indicates that a borrow or carry out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during shift and rotate operations and the execution of SET_BCF, CLR_BCF and CCR! instructions.

Zero (Z)

When the bit is set, it indicates that the result of the last arithmetic or logical manipulation was zero.

Branch (B)

A conditional branch takes place when the branch flag was set by one of the previous instructions (e.g., a comparison operation).

Instructions such as SET_BCF, TOG_BF and CLR_BCF allow the direct manipulation of the branch flag under program control. The flag is affected by all ALU operations except CCR@, DI, SWI, RTI and OUT.

Interrupt Enable (I)

This flag is used to interrupt processing on global basis. Resetting the interrupt enable flag (using the DI instruction) disables all interrupts. The µC does not process further interrupt requests until the interrupt enable flag is set again by either executing an EI, RTI (return-from-interrupt) instruction or entering the SLEEP mode. After power-on or an external reset the interrupt enable flag is automatically reset. The RTI instruction at the end of the $RESET routine will set the interrupt enable flag and thereby enable all interrupts.

2.3.7 Self-Check

The self test capability of the MARC4 provides the possibility of checking the core, ROM, RAM, interrupt and prescaler easily. The $RESET routine (after power-on reset) allows to choose the test routine or the application program.

Note: The necessary test routine were delivered by TEMIC.

3 Reset Modes, Interrupts, Prescaler and Low Power Modes

3.1 Reset Modes

The M43C200 has three reset modes: an active low external reset pin (RST), a power-on and an oscillator watchdog reset function.

3.1.1 External Reset (NRST)

The external reset (NRST) input pin is used to provide an orderly software startup procedure of the µC. When using the external reset mode, the RST pin should be low for a minimum of two instruction cycle times (typically 4 µs). The pin RST has an internal pull-up.

3.1.2 Power-on Reset

The power-on reset occurs when a positive transition is detected on the power supply input. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. A power-down reset occurs when a negative transition is detected on the power supply input for 5 ms or more. To improve noise immunity the power-on reset has Schmitt-trigger characteristics as shown in figure 8.

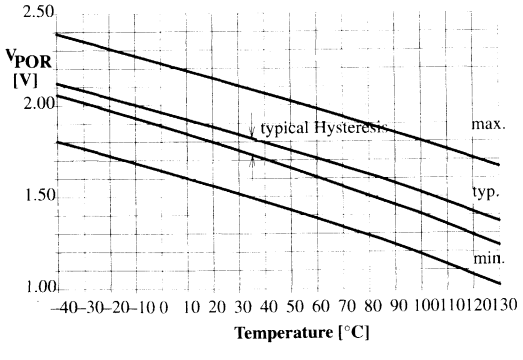


Figure 8. Temperature versus V_{POR}

3.1.3 Oscillator – Watchdog Reset Function

The oscillator-watchdog guarantee a well-defined clock condition by using a quartz or a ceramic resonator.

After starting, normally this sorts of oscillator generates undefined clock signals. In this case the amplitude is controlled by the oscillator-watchdog. When the right value of oscillator-amplitude is detected the RST-pin will be hold LOW for 32 oscillator periods. After this time the µC starts the $RESET routine.

When extern clock is used (pin OSCOUT as clock input) the amplitude must be 0.9 × V_{DD} otherwise the oscillator watchdog will detect an error.

3.1.4 Effects on Internal Circuitry

All reset modes guarantee a well-defined start condition of the complete microcontroller. During RESET all interrupts are disabled, all pending and active interrupts are cleared, all on-chip peripherals are reset and a non-maskable interrupt request is generated. The RESET has the absolute highest priority, having access to the microcontroller at all times.

	Function	Located in ROM at	Max. Length [ROM bytes]	Interrupt Opcode
$RESET	Software & hardware initialization	008 h	56	C1 h

The main tasks of the reset service routine ($RESET) are:

- Stack pointer initialization,
- Variable and array initialization, and
- Initialisation and setup of the peripherals.

After execution of the reset service routine, the interrupts are enabled automatically by the RTI or previously executed EI instruction.

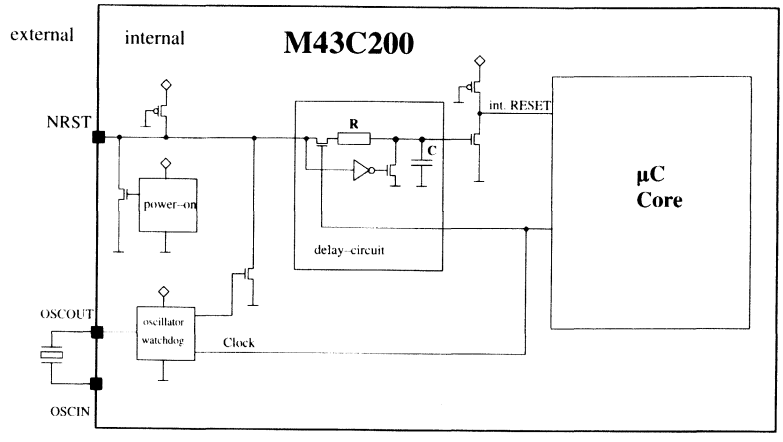


Figure 9. Reset functions

3.1.5 Summary of all Reset Functions

Figure 9 shows all reset functions: external NRST, power-on and oscillator-watchdog. All these resets will generate an internal reset after passing the delay circuit. Normally the delay time is about 40 periods of the system frequency (TCL).

3.2 Interrupts

The M43C200 can handle interrupts of 8 priority levels (table 1). They are generated from on-chip modules (prescaler), external sources (port 5 and interrupt pad) or synchronously from the core itself (software interrupts). Each interrupt source has a hard-wired interrupt priority and an associated interrupt service routine in the program ROM. The programmer can enable or disable all interrupts by setting or resetting the interrupt enable flag in the CCR using the EI or DI instruction.

When the interrupt enable flag is reset (interrupts disabled), the execution of interrupts is inhibited but not the logging of the interrupt requests in the interrupt pending register. While interrupts are disabled (e.g., for a time critical section of code) and an interrupt is generated the interrupt will not be lost. Its execution will only be delayed until interrupts are enabled again. Interrupts are only lost when the pending register for a particular interrupt priority is still set at the time of a further interrupt transmission of the same level. The pending resister is reset either on power-on reset or on compilation of corresponding interrupt service routine by execution the RTI instruction (see figures 10 and 11).

The µC automatically enters the SLEEP mode when the lowest priority interrupt service routine has been completed. This guarantees a maximum use of the power saving capabilities of the µC. For further information please refer to low power modes.

Table 1. Interrupt priority and address allocation map

Priority	Function	Located in ROM at	Max. Length [ROM bytes]	Interrupt Opcode
INT7	Software interrupt	1E0h	> 24	**FCh**
INT6	Software interrupt	1C0h	32	**F8h**
INT5	Software interrupt	180h	64	**F0h**
INT4	Prescaler interrupt	140h	64	**E8h**
INT3	External hardware interrupt negative edge triggered	100h	64	**E0h**
INT2	Software interrupt	0C0h	64	**D8h**
INT1	External hardware interrupt negative edge triggered (port 50, 51, 52)	080h	64	**D0h**
INT0	Software interrupt	040h	64	**C8h**

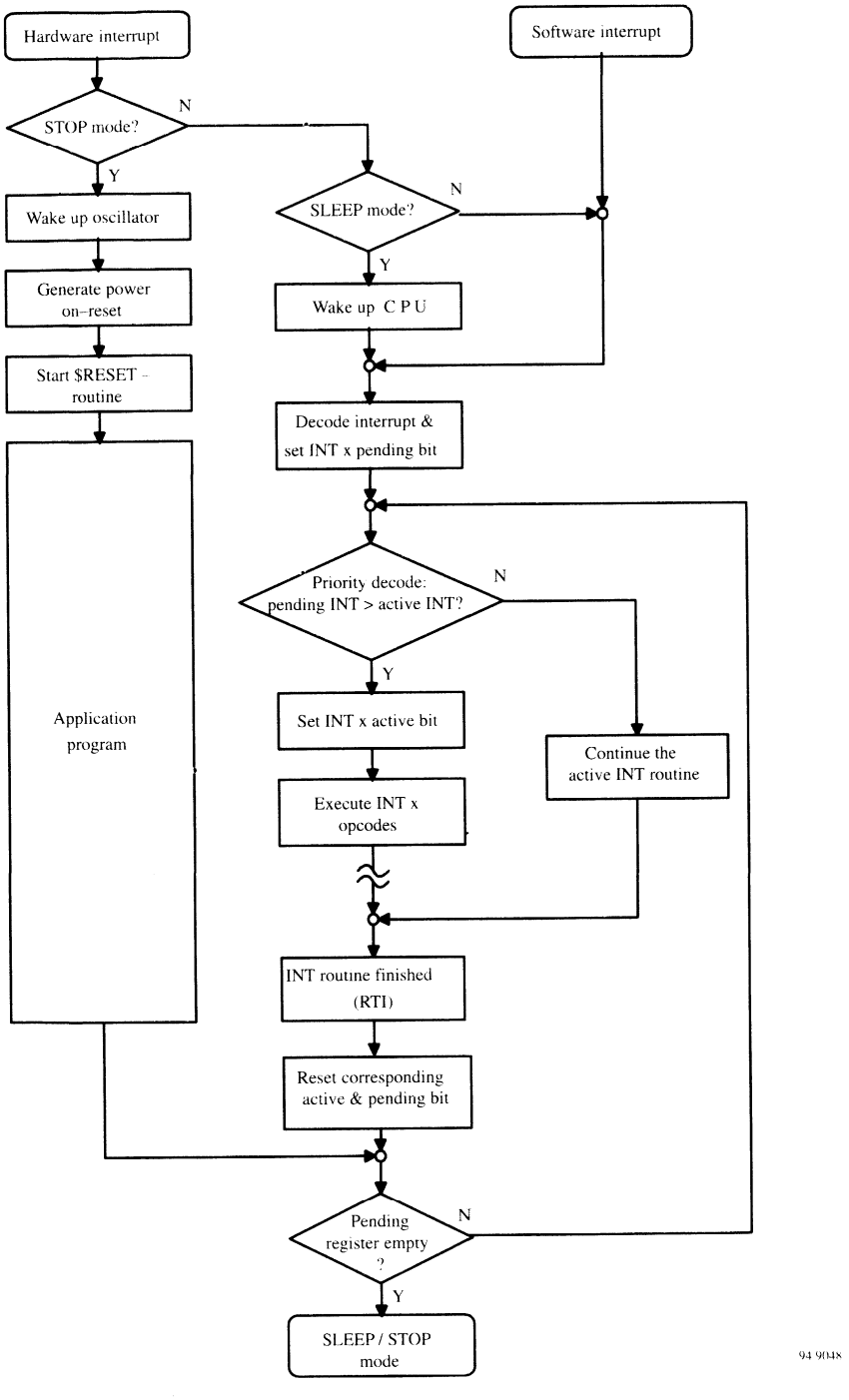


Figure 10. Interrupt flow chart

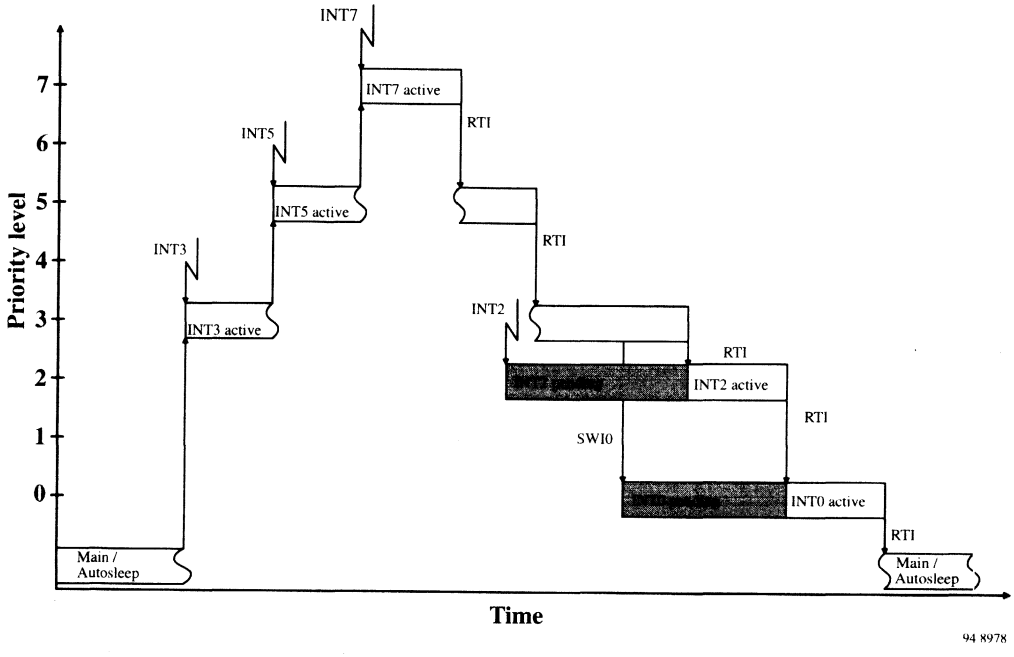


Figure 11. Interrupt handling

3.2.1 Interrupt Handling

The integrated interrupt controller samples all interrupt requests and latches these in the interrupt pending register. It also decodes the priority of the interrupt requests, and signals the µC when a higher priority interrupt requests is present. If the µC (with interrupts enabled) receives the interrupt controller's signal, an interrupt acknowledge cycle will be entered. During this cycle, the µC saves the current PC on the return stack and loads the PC with the start address of the corresponding interrupt service routine. When the µC is in the SLEEP mode, it will be activated by any hardware interrupt, by the means of wake-up the CPU and decoding the interrupt.

Using the MARC4 way of interrupt transmission, it is possible to transmit more than one interrupt at the same time. The transmitted interrupts are loaded into the interrupt pending register asynchronously. The priority decoder determines the interrupt with the highest priority and activates it as shown in figure 11.

If the µC was in stop-mode any interrupt will start the oscillator. This will generate a reset and starts the $RESET routine.

3.2.2 Interrupt Latency

The interrupt latency is the time from the falling edge of the interrupt to the interrupt service routine being activated. This time is between three or five instruction cycles depending on the state of the core. The highest frequency which can be reasonably handled on the duty cycle of the application.

3.2.3 Software Interrupts

Software interrupts are executable instructions which are supported by predefined macros named SWI 0 through SWI 7. The software triggered interrupts operates exactly like any hardware triggered interrupt.

3.2.4 Hardware Interrupts

Port 5 interrupt

Any of the input port 50, 51 and 52 may generate an interrupt level 1 (see figure 5). The INT1 is negative edge triggered and has Schmitt-trigger characteristics.

External interrupt

The external interrupt INT3 is negative edge triggered and has Schmitt-trigger characteristics to improve the noise immunity (see figure 12).

Figure 12. External interrupt input

3.3 Prescaler Interrupt

The programmable prescaler is usually driven by an internal frequency of 31.25 kHz. The prescaler consists of a stage divider chain. This divider chain offers an interrupt source with the priority level 4. The prescaler module powers up in the reset condition which corresponds to control code Fh. The prescaler interrupt (INT4) has 15 programmable taps from 15.625 kHz down to 1 Hz. They are selectable by writing a value of E...0 into the control register at port address 15.

3.3.1 Prescaler During SLEEP Mode

When the microcontroller enters the SLEEP mode, the core clocks are halted. While the 4 MHz oscillator and prescaler remain active, all µC actions are suspended. The microcontroller exists in the SLEEP mode when an interrupt is generated by the prescaler (in addition to a logic low on an external interrupt (INT3), port 50, 51, 52 input pin (INT1), or an external reset).

3.4 Low Power Modes

Two low power consumption modes of operation are available: SLEEP and STOP mode. These operating modes are initiated by executing the SLEEP instruction.

Note: The SLEEP instruction is not a normal instruction as its function is depended on the state of the interrupt pending register. SLEEP is therefore available for use within the $AUTOSLEEP routine only.

3.4.1 SLEEP Mode

By executing the SLEEP instruction (in the $AUTOSLEEP routine) the microcontroller enters a low power consumption mode. In this SLEEP mode, the programmable prescaler remains active, while the internal µC clock is turned off causing all core processing to be stopped. It can only be kept when none of the interrupt pending or active register bits are set.

Table 2. Selectable interval times for the prescaler

Control Code Port Address 15	Interrupt Frequency f_C / n	f_C = 31.25 kHz Time Interval
F		reset & hold complete prescaler
E	$n = 2^1$	64 µs
D	$n = 2^2$	128 µs
C	$n = 2^3$	256 µs
B	$n = 2^4$	512 µs
A	$n = 2^5$	1.024 ms
9	$n = 2^6$	2.048 ms
8	$n = 2^7$	4.096 ms
7	$n = 2^8$	8.192 ms
6	$n = 2^9$	16.384 ms
5	$n = 2^{10}$	32.769 ms
4	$n = 2^{11}$	65.536 ms
3	$n = 2^{12}$	131.072 ms
2	$n = 2^{13}$	262.144 ms
1	$n = 2^{14}$	524.288 ms
0	$n = 2^{15}$	1.048 s

During the SLEEP mode, the I bit in the condition code register (CCR) is set to enable all interrupts. All other registers, memory, and parallel input/output lines remain the same. The 4 MHz oscillator is not switched off, but the prescaler may be disabled by the application program. This mode will continue until any interrupt or reset is sensed. At this time the event is decoded and the program counter is loaded with the corresponding starting address of the interrupt or reset service routine.

The MARC4 unique AUTOSLEEP feature allows the µC to enter the SLEEP mode automatically when the lowest priority interrupt service routine has been completed.

The SLEEP mode is a shutdown condition which is used to reduce the average system power consumption in applications where the µC is not fully utilised (figure 13). Using SLEEP and interrupts, the full computational speed of the core is always available. In this way, power is only consumed when needed, allowing the µC to run in high speed bursts from a weak supply (battery, capacitor, or even a solar cell).

Calculating the average power consumption

The total power consumption is directly proportional to the active time of the µC. For a rough estimation of the expected average system current consumption, the following formula should be used:

$$I_{SYS} = I_{SLE} + (I_{DD} * T_{active}/T_{total})$$

3.4.2 STOP Mode

The lowest power consumption mode of the microcontroller is entered with the STOP operation. The current consumption of the µC (without external loads) will be reduced to 1 µA.

The STOP mode can be implemented by switching off power supply of 4 MHz oscillator. This can be done with a combination of INRUN (BP42 "L") and SLEEP.

During the STOP mode, the I bit in the CCR is set to enable external interrupts. All other registers, memory, and all I/O lines remain unchanged. This continues until an external interrupt or reset is decoded. After an external interrupt or reset the 4 MHz oscillator starts and generates a reset signal. The program counter is loaded with the reset service routine.

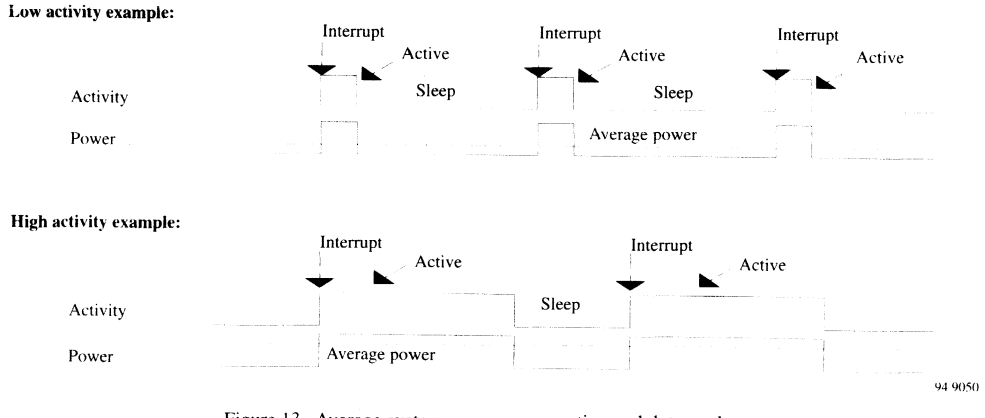


Figure 13. Average system power consumption and duty cycle

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

All voltage are given to V_{SS}.
The circuit is protected against supply voltage reversal for 5 minutes typically @I_{max} = 100 mA.

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage (on any pin)	V_{IN}	V_{SS} –0.3 ≤ V_{IN} ≤ V_{DD} +0.3	V
Output short circuit duration	t_{short}	indefinite	s
Operating temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	T_{stg}	–40 to +130	°C
Thermal resistance (PLCC)	R_{thJA}	110	K/W
Soldering temperature (t ≤ 10 s)	T_{sd}	260	°C

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device is required. All inputs and outputs are highly protected against electrostatic discharges. However, precautions to minimize the built-up of electrostatic charges during handling.

For proper operation it is recommended that V_{IN} and V_{OUT} be limited to the range:

$$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$$

If in the applications pin 1 (INT3) is not used it must be connected to V_{DD}.

4.2 DC Operating Characteristics

Supply voltage V_{DD} = 2.4 to 6.2 V, V_{SS} = 0 V, T_{amb} = +25°C unless otherwise specified

4.2.1 Supply Currents

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current active mode	V_{DD} = 2.4 V	I_{DD}		0.5	0.7	mA
	V_{DD} = 6.2 V			2.7	3.2	mA
Supply current SLEEP mode	V_{DD} = 2.4 V	I_{SLE}		100	130	µA
	V_{DD} = 6.2 V			600	750	µA
Supply current STOP mode	V_{DD} = 2.4 V	I_{STP}		0.08	0.5	µA
	V_{DD} = 6.2 V			0.5	0.8	µA

Input voltage pad OD, NRST, TE, port 0, 1, 4, 5

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Input voltage LOW	V_{DD} = 2.4 – 6.2 V	V_{IL}	V_{SS}		0.2 × V_{DD}	V
Input voltage HIGH	V_{DD} = 2.4 – 6.2 V	V_{IH}	0.8 × V_{DD}		V_{DD}	V

4.2.2 Power-on Reset (POR)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
POR voltage		V_{POR}	1.5		2.13	V
POR voltage hysteresis		V_{POR}		100		mV

4.2.3 DC Electrical Characteristics, V_{DD} = 2.4 V @ 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Pad OD, NRST						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–0.8		–5.3	µA
Pad TE						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	1.1		5.0	µA
Bidirectional ports 0.0 – 0.3, 1.0 – 1.2, 4.2 and 4.3						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	1.1		5.0	µA
Output current n-channel pull-down	$V_{OL} = V_{SS}$ +0.5 V	I_{OL}	0.7		2.6	mA
Output current p-channel pull-up	$V_{OH} = V_{DD}$ –0.5 V	I_{OH}	–0.6		–2.0	mA
Bidirectional port 1.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–0.8		–5.3	µA
Output current n-channel pull-down	$V_{OL} = V_{SS}$ +0.5 V	I_{OL}	0.7		2.6	mA
Output current p-channel pull-up	$V_{OH} = V_{DD}$ –0.5 V	I_{OH}	–0.6		–2.0	mA
Input port 5.0 – 5.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–6.1		–38.2	µA

4.2.4 DC Electrical Characteristics, V_{DD} = 6.2 V @ 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Pad OD, NRST						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–8.0		–51.0	µA
Pad TE						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	8.2		36.2	µA
Bidirectional ports 0.0 – 0.3, 1.0 – 1.2, 4.2 and 4.3						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	8.2		36.2	µA

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Output current n-channel pull-down	$V_{OL} = V_{SS} + 1.3$ V	I_{OL}	5.0		13.0	mA
Output current p-channel pull-up	$V_{OH} = V_{DD} - 1.3$ V	I_{OH}	–5.0		–14.0	mA
Bidirectional port 1.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–8.0		–51	µA
Output current n-channel pull-down	$V_{OL} = V_{SS} + 1.3$ V	I_{OL}	5.0		13.0	mA
Output current p-channel pull-up	$V_{OH} = V_{DD} - 1.3$ V	I_{OH}	–5.0		–14.0	mA
Input port 5.0 – 5.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–58		–366	µA

4.2.5 Oscillator

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Frequency	C_L = 1 pF	f		4.0		MHz
Integrated input capacitance		C_{IN}		10		pF
Integrated output capacitance		C_{OUT}		10		pF
Start-up time quartz	V_{DD} = 2.4 V *)	t_{SQ}		8	90	ms
	V_{DD} = 3.0 V *)			4.5	10	ms
	V_{DD} = 5.0 V *)			2.5	4	ms
Start-up time ceramic	V_{DD} = 2.4 V **)	t_{SC}		250	—	µs
	V_{DD} = 3.0 V **)			150	300	µs
	V_{DD} = 5.0 V **)			150	160	µs

*) Measured with a typical quartz
C_1 = 3.2 fF
L_1 = 490 mH
R_1 = 40
C_0 = 1.4 pF

**) Ceramic
C_1 = 4.4 pF
L_1 = 385 µH
R_1 = 8.2
C_0 = 36.3 pF

4.3 I/O Port Characteristics

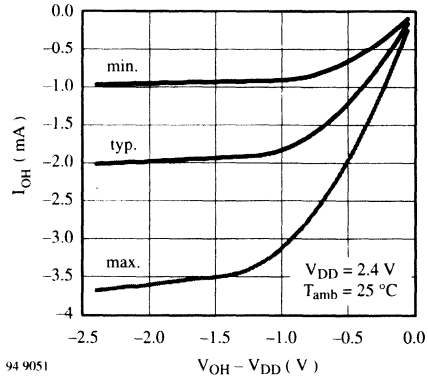


Figure 14. P-channel source current

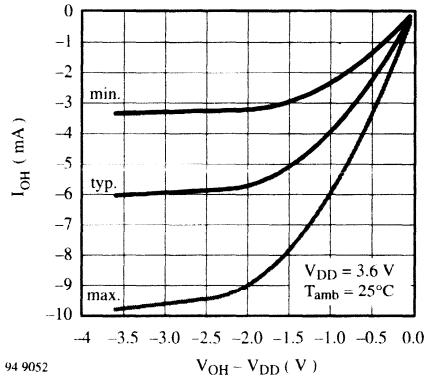


Figure 15. P-channel source current

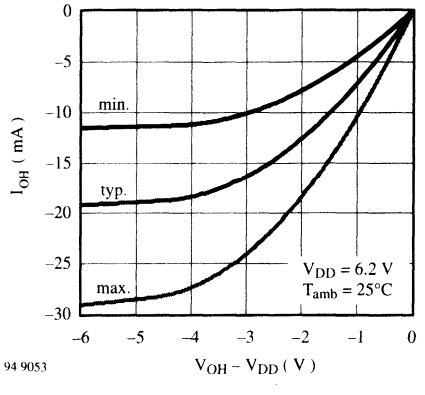


Figure 16. P-channel source current

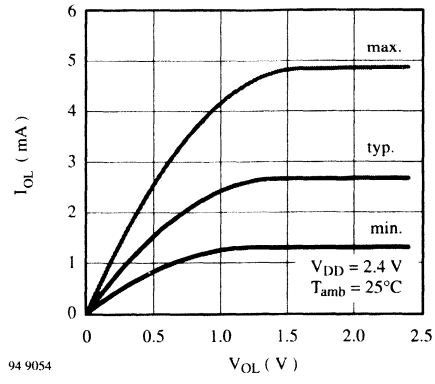


Figure 17. N-channel sink current

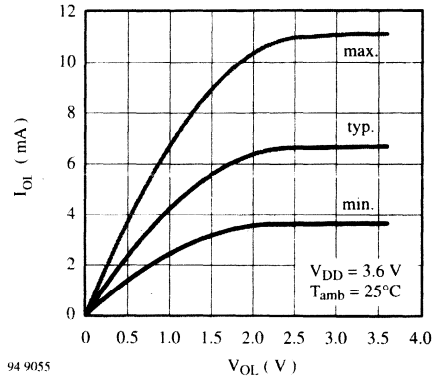


Figure 18. N-channel sink current

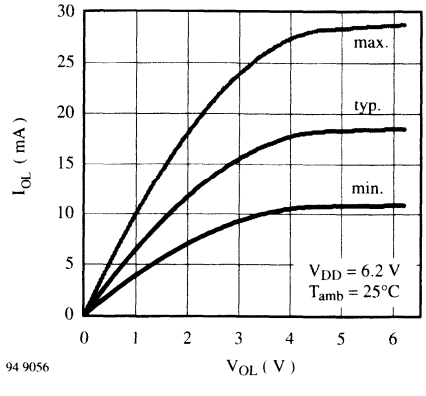


Figure 19. N-channel sink current

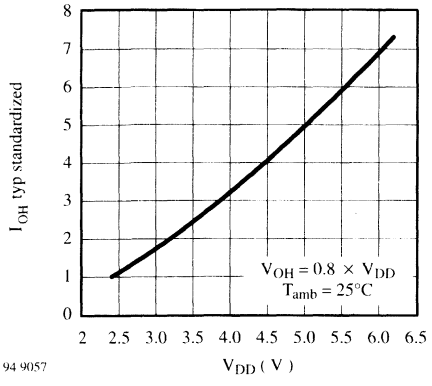


Figure 20. Standardized p-channel source vs. V_{DD}

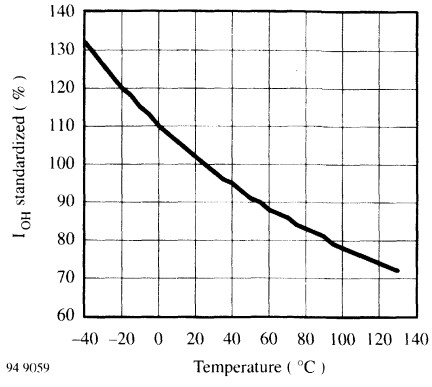


Figure 22. Standardized p-channel source current vs. ambient temperature

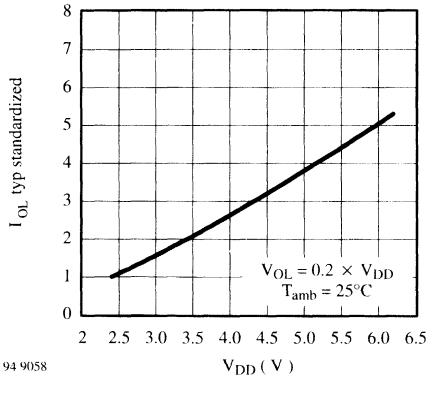


Figure 21. Standardized n-channel sink current vs. V_{DD}

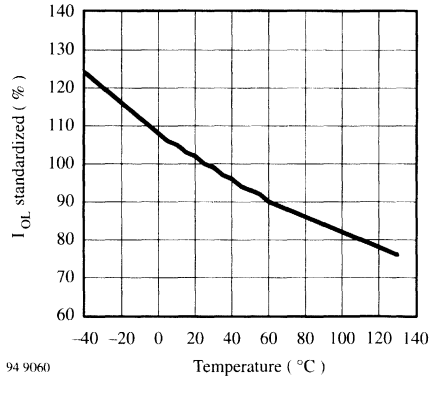


Figure 23. Standardized n-channel sink current vs. ambient temperature

4.4 Characteristics of the Pull-Up and Pull-Down Transistors

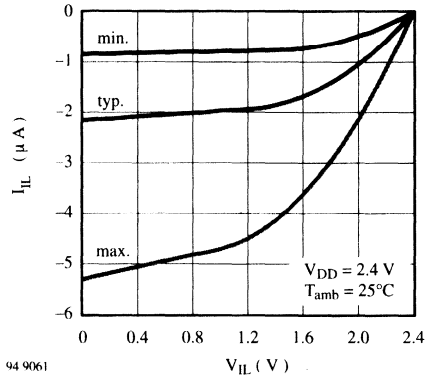


Figure 24. PIN OD: p-channel source current

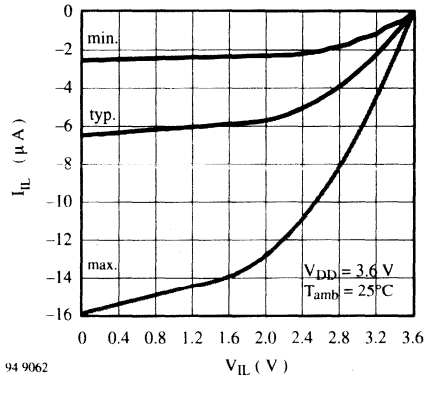


Figure 25. PIN OD: p-channel source current

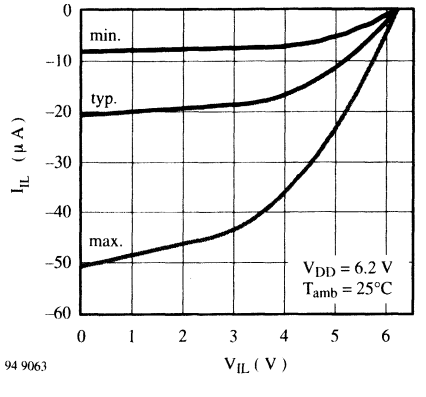


Figure 26. PIN OD: p-channel source current

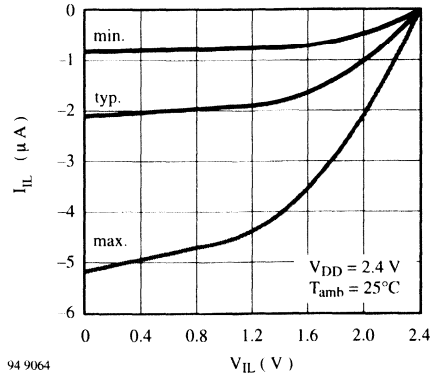


Figure 27. PIN NRST: p-channel source current

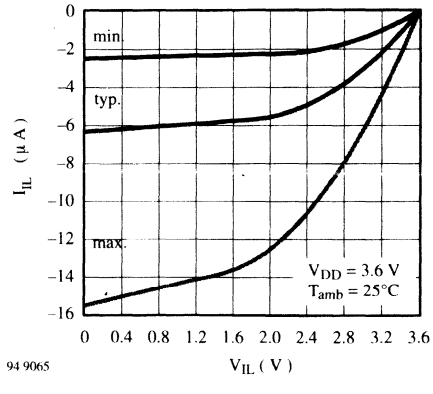


Figure 28. PIN NRST: p-channel source current

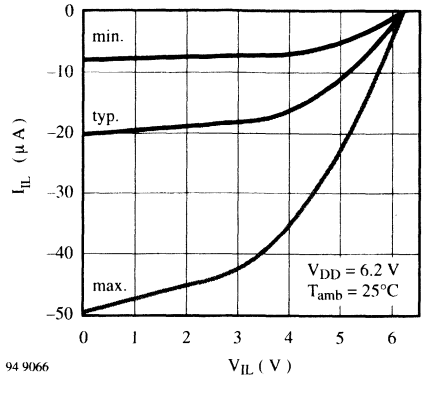


Figure 29. PIN NRST: p-channel source current

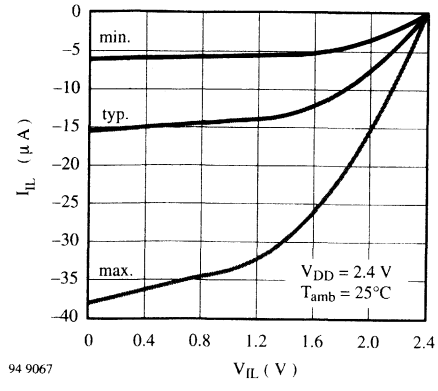


Figure 30. PIN IP5x: p-channel source current

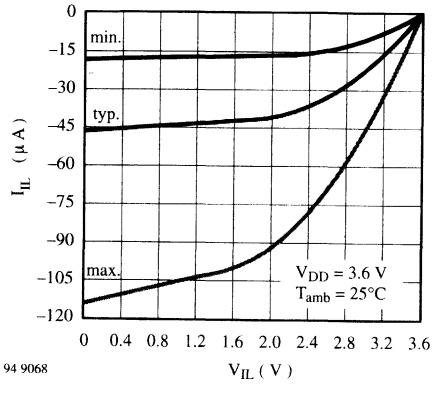


Figure 31. PIN IP5x: p-channel source current

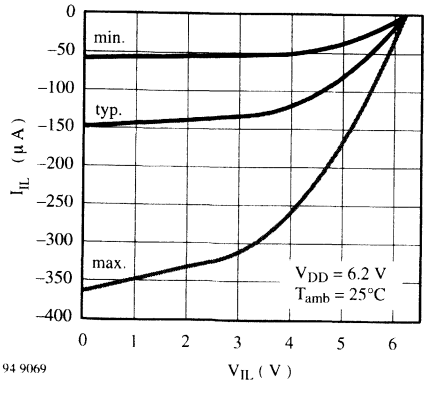


Figure 32. PIN IP5x: p-channel source current

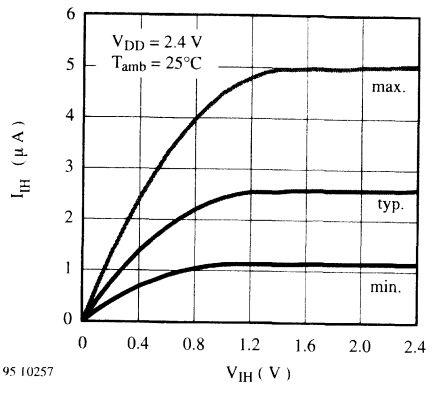


Figure 33. All PINs with pull-down: n-channel sink current

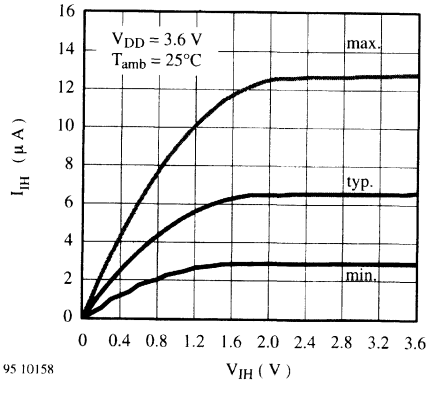


Figure 34. All PINs with pull-down: n-channel sink current

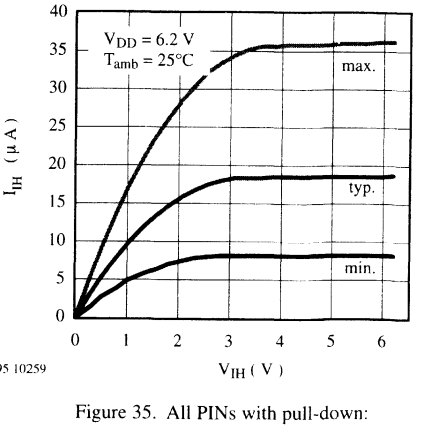


Figure 35. All PINs with pull-down: n-channel sink current

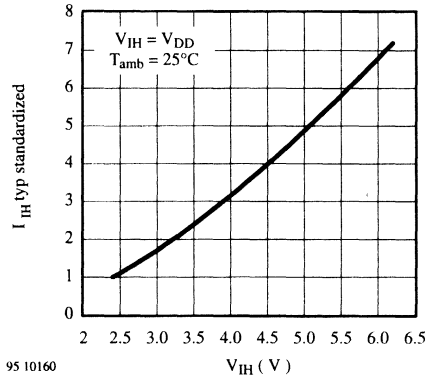


Figure 36. Standardized p-channel source current vs. V_{DD}

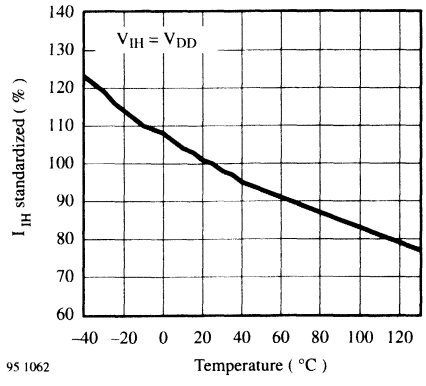


Figure 38. Standardized p-channel source current vs. ambient temperature

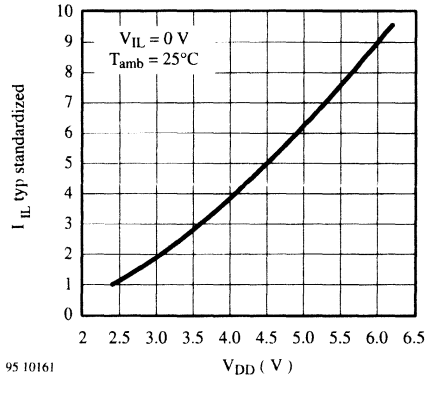


Figure 37. Standardized n-channel sink current vs. V_{DD}

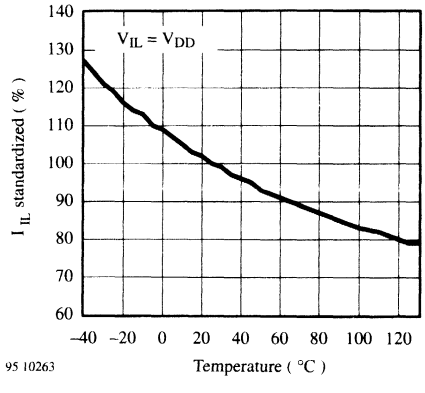
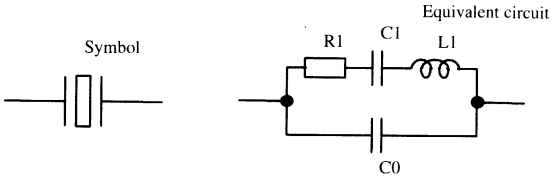


Figure 39. Standardized n-channel sink current vs. ambient temperature

5 Characteristics of the On-Chip Quartz / Ceramic Oscillator

Equivalent Circuit of the Quartz and Ceramic Resonator



The criteria for oscillation depends on R1 and C0. Following diagrams show the equivalent quartz circuits over temperature range –40 to +125°C for two different values of V_{DD}. The figure below shows the maximal values of the equivalent circuit of the ceramic-resonator for start up at V_{DD} = 3.0 V and ambient temperature range from –40 to +125°C. For this test a resonator CSAC4.00 (MURATA) was used.

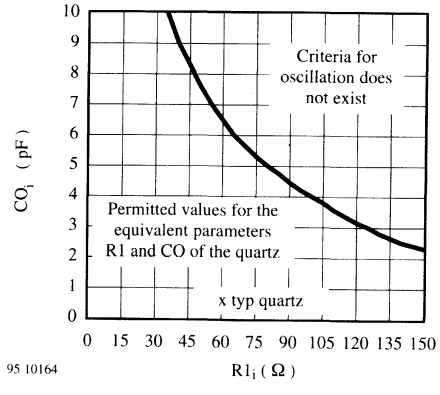


Figure 40. V_{DD} = 2.4 V

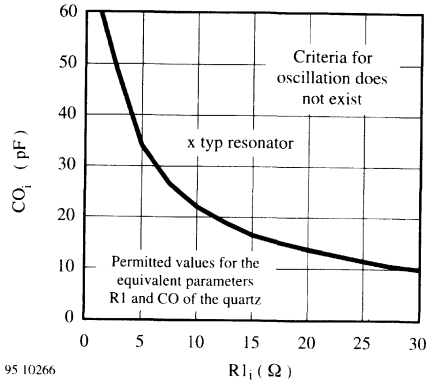


Figure 42. V_{DD} = 2.4 V

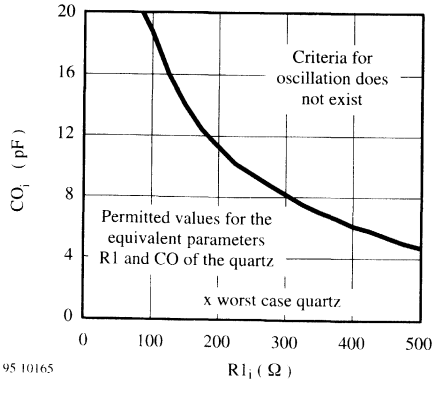


Figure 41. V_{DD} = 3.0 V

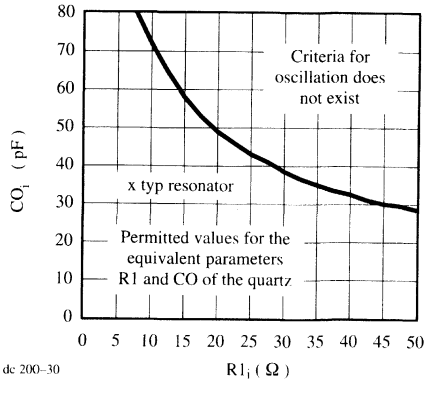


Figure 43. V_{DD} = 3.0 V

Note: For pc-board design place the quartz or ceramic resonator nearby the pins because of low parasitic capacities (≤ 0.5 pF).

6 Characteristics of the Schmitt Trigger Inputs

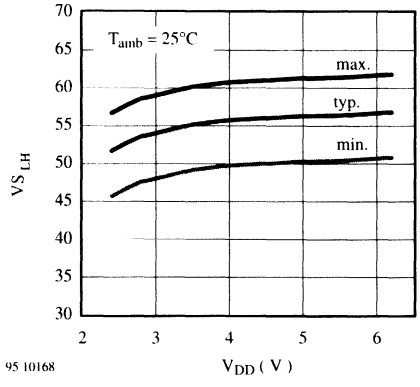


Figure 44. Voltage switch level for positive edge trigger vs. V_{DD}

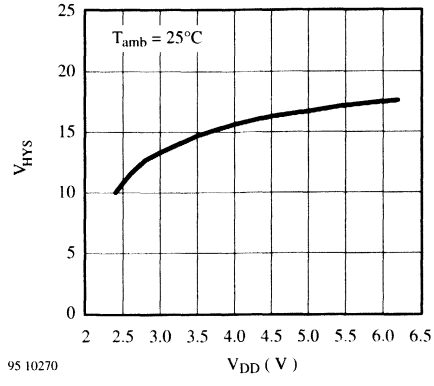


Figure 46. Hystereses in percent of supply voltage vs. V_{DD}

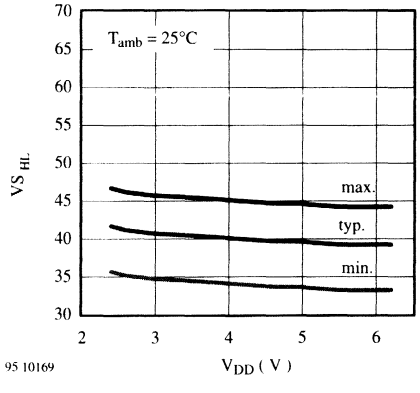


Figure 45. Voltage switch level for negative edge trigger vs. V_{DD}

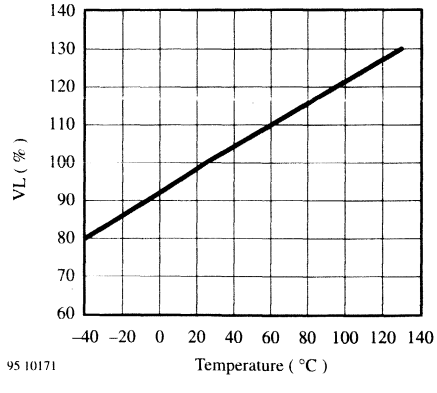


Figure 47. Typical switch level vs. ambient temperature

Note: The values of min., typ. and max. for the positive or negative edge trigger are matched.

Note: For recognize a input pulse a minimum pulse time of 50 ns is necessary. The transition time must be ≤ 10 ns.

7 Ordering Information

Pin options

Please select the option setting from the list below.

Pin	Output		Input	
	CMOS	Open Drain	Pull-Up	Pull-Down
BP00				
BP01				
BP02				
BP03				
BP10				
BP11				
BP12				
BP13				
BP20				
BP21				
BP22				
BP23				
BP30				
BP31				
BP32				
BP33				
IP40–INT6				
IP41–TA				
IP42–TB				
IP43				
NWP				
TE				

ROM code

Please insert ROM CRC.

Size: _____ KByte **CRC:** _____ hex

Approval

Date: _____ Signature: _____

MARC4 – 4-bit Microcontroller

The M43C201 is a member of the TEMIC family of 4-bit single chip microcontroller. It contains ROM, RAM, parallel I/O ports and on-chip clock generation.

Features

- **Stack oriented HARVARD architecture**
  - 4K × 8-bit ROM
  - 256 × 4-bit RAM
  - 2 µs instruction cycle @ 4 MHz OSC-frequency
- **Programming**
  - User friendly in high level language qFORTH
- **Development system**
  - PC-based
  - Highly optimising compiler
- **Low power**
  - STOP mode @ 1 µA
  - SLEEP mode typically 500 µA
  - RUN mode typically 3 mA
- **High operating range**
  - Supply voltage range 2.4 to 6.2 V
  - Temperature range –40 to 85°C
- **Interrupt structure**
  - 1 prescaler/timer interrupt
  - Software interrupts
  - Autosleep

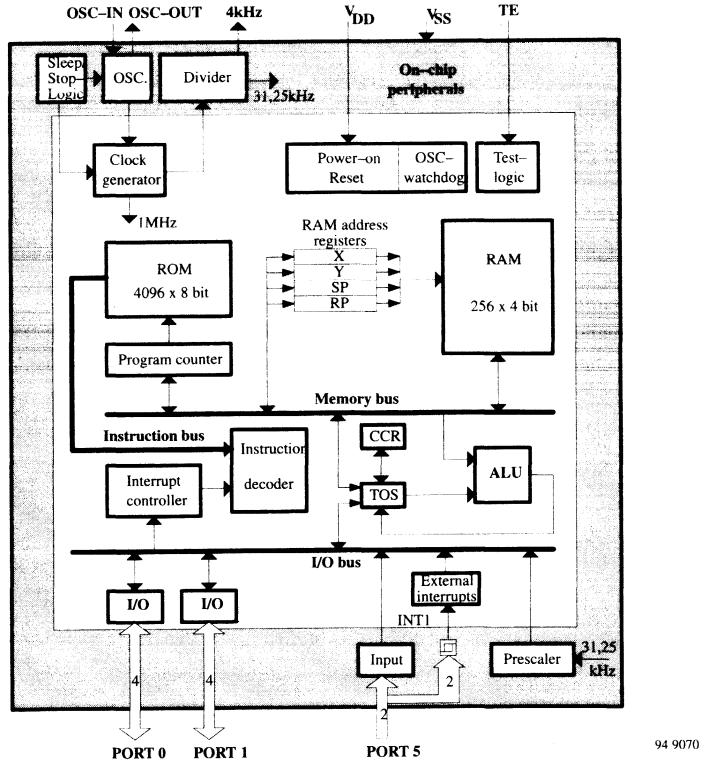


Figure 1. Functional block diagram

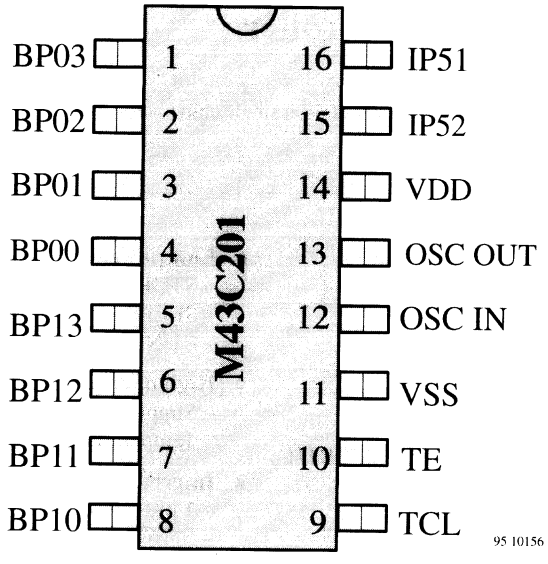


Figure 2. Pin assignment SO16 (top view)

Table 1. Pin description

Name	Function
V_{DD}	Power supply voltage 2.4 to 6.2 V
V_{SS}	Circuit ground
BP00 – BP03	4 bidirectional I/O lines of port 0 *
BP10 – BP13	4 bidirectional I/O lines of port 1 *
IP50 – IP51	2 input lines of port 5
OSCIN	Oscillator input (32-kHz crystal)
OSCOUT	Oscillator output (32-kHz crystal)
TCL	External system clock I/O. This pin can be used as input to provide the C with an external clock.
TE	Testmode input. This input is used to control the test modes and the function of the TCL pin.

*) The I/O ports have CMOS output buffers. As input they are available with pull-up or pull-down resistors. Please see the order information.

Note: For emulation use the M43C200 type in a SO24 case.

Table of Contents

Table of Contents (continued)

1 General Description

The M43C201 is a member of the TEMIC MARC4 family (single chip **M**odular **ARC**hitecture **4**-bit microcomputers). It contains ROM, RAM, I/O ports, 15 stage prescaler, 4 MHz oscillator and 2 external interrupts.

Note: About 0.5 Kbyte of the 4 K ROM are required for the self-test program.

The CPU is built around a stack based Harvard type architecture, where the program memory (in ROM) and the data memory (in RAM) are physically separated and addressed independently.

The M43C201 has a typical instruction cycle time of 2 µs @ 4 MHz oscillator frequency.

The SLEEP instruction allows the CPU to be stopped by the program, thereby enabling reduction in current consumption. Once the CPU has entered SLEEP mode it can be revived into active state immediately, following the receipt of an interrupt. In SLEEP mode, the CPU is held in a defined state whereby all data are latched. In the SLEEP mode the 4-MHz oscillator and the prescaler/ timer are still running. It gives the opportunity to wake up the CPU in a defined time which is given by the prescaler.

The highest power saving mode is the STOP mode. In this case the CPU, oscillator and prescaler are all stopped controlled by the internal NRUN signal. If an interrupt appears the 4-MHz oscillator will be started, controlled by the SLEEP/STOP logic. When the oscillator has reached the exact frequency a reset is generated and the program will start the $RESET routine.

1.1 Interrupt Structure

The MARC4 can handle up to 8 priority interrupts which can be generated from on-chip modules (prescaler), external sources (interrupt pad) or synchronously from the CPU itself (software interrupts).

An additional power-on reset interrupt is used for initialising the CPU. The purpose of the power-on reset is to start the oscillator and to put the CPU into a well defined condition after the operating voltage has been reached. The reset interrupt has the absolute highest priority having access to the CPU at all times. The processor will automatically enter SLEEP when the lowest priority task has been completed, so making maximum use of the power saving capabilities of the MARC4.

1.2 Prescaler

A programmable prescaler driven by 31.25 kHz offers 1 interrupt. Table 2 (page 142) illustrates the eligible interrupt frequencies. The prescaler powers up in the reset condition.

2 Pin-, Signal-, Memory-, Core Registers- and Self-Check Description

2.1 Pin Description

2.1.1 V_{DD}, V_{SS}

V_{DD} is the power for the µC core, RAM, ROM and the peripherals, V_{SS} is ground.

2.1.2 TCL

The system clock for the microprocessor is derived from a fully integrated on-chip crystal oscillator circuit. This oscillator tracks the supply and temperature to ensure optimum operation of the microcontroller under all conditions.

The TCL pin is necessary as clock input for the test- and emulation mode.

2.1.3 TE

These line is needed for test and emulation.

2.1.4 OSCIN, OSCOUT

An oscillator with a divider stage is integrated in the chip to generate the 1 MHz clock frequency (TCL). This oscillator is operated by simple connection of 4 MHz quartz or ceramic resonator.

This oscillator can be controlled via port 42 (NRUN-signal). This means that the oscillator can be stopped in SLEEP mode or remains active if operation of the prescaler is desired. However, this function can only be set by software.

INRUN – signal "high"
the µC goes in sleep mode after finishing the lowest (Port 42) interrupt (oscillator running).

INRUN – signal "low"
the µC goes in STOP mode after finishing the lowest interrupt (oscillator stop).

2.1.5 Bidirectional Ports

Port 0 and 1 may be programmed as an input or an output under software control. The direction of a port is determined by an IN or OUT instruction and is held until another IN or OUT instruction for this port is executed.

The direction of this bidirectional ports is not switchable on a bit-wise basis. The output latches hold the state of last data value written to the port. At power-on or external reset all pins of port 0 and 1 are set to input mode and all output latches are set to a logic 1.

Whenever the port is switched from input to output the last value stored in the latches will appear on the outputs for one clock cycle (figure 4).

When switching bidirectional ports from output to input the stray capacitance of the connection wires may cause the data read to be the same as the last data written to this port. This behaviour can be used by connecting large enough capacitors to the pins of the bidirectional port to read back the previous data written to this port.

On the other hand, to avoid the negative effects of stray capacitance the following approaches should be used:
Use two IN instructions, and DROP the first data nibble read.

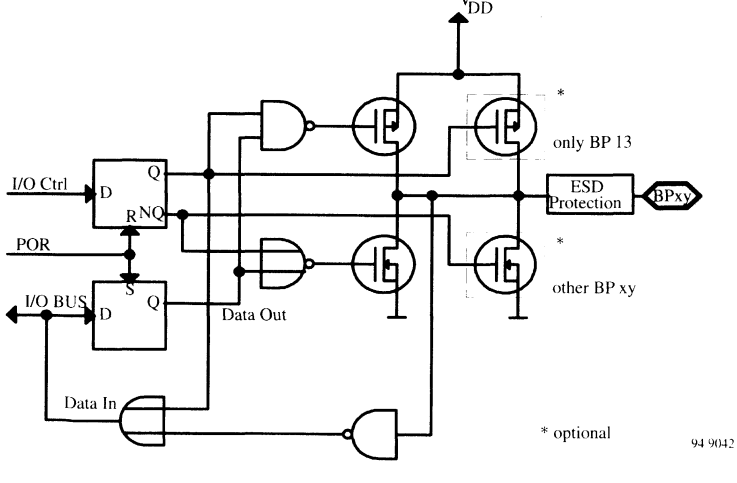
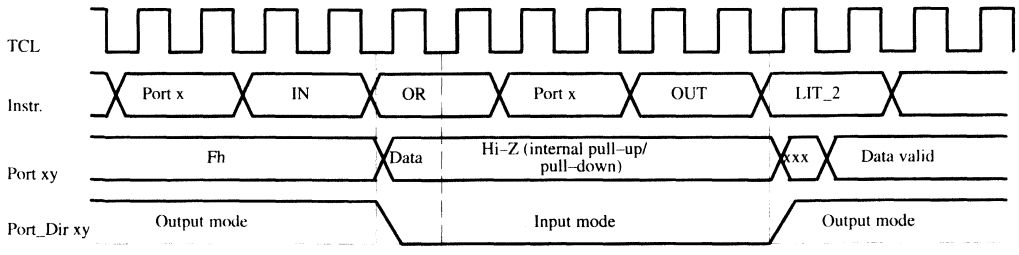


Figure 3. Bidictional port schematics



xxx) Last written data contained in output latches, Fh after power-on-reset

Figure 4. Read and write cycle timing

2.1.6 Input Port 5

The data on port 5 is sent to the top of the expression stack whenever an IN instruction (addressing port 5) is executed. The pins IP51 and IP52 of the port 5 may generate an additional interrupt (priority level 1), when any of the three input lines is driven low. This function is useful for implementing an interrupt driven keyboard. The interrupt lines are negative edge triggered and have Schmitt-trigger characteristics to improve the noise immunity. The interrupt function is enabled after power-on or external reset. This interrupt can be disabled by software.

2.2 Memory

The MARC4 family of microcontroller is based on the Harvard architecture with physically separate program memory (ROM) and data memory (RAM).

The program memory (ROM) is mask programmed with the customer application program during the fabrication of the microcontroller. The ROM is addressed by a 12-bit wide program counter, thus limiting the program size to a maximum of 4096 bytes which cannot be extended by using external memory. The user ROM starts with a 512 byte segment ('Zero Page') which contains predefined start addresses for interrupt service routines and special subroutines accessible with single byte (SCALL) instructions. The corresponding memory map is shown in figure 6.

The self test routines should be included as part of the free program space. The 16-bit check sum (CRC) is located by the compiler in the last two bytes of ROM.

The on-chip 256 × 4-bit RAM is divided in the 12-bit wide return stack, the 4-bit wide expression stack (both with a user definable depth) and the data memory. The fixed return address (00h) which points to the $AUTOSLEEP routine is located at RAM address FCh.

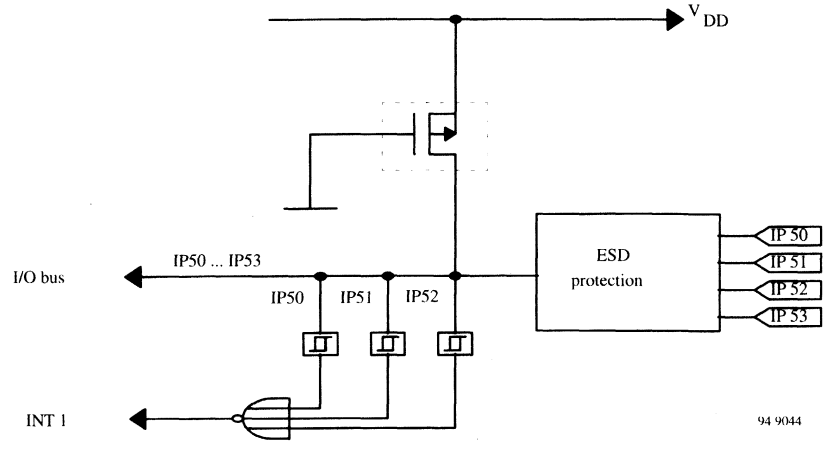


Figure 5. Input port

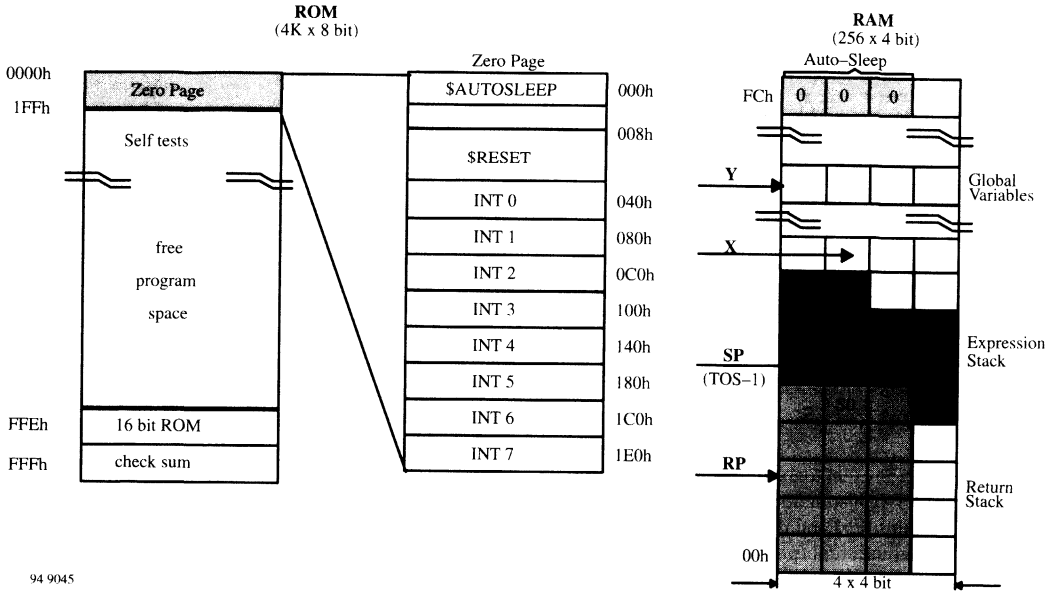


Figure 6. Memory map

2.3 Core Registers

As shown in the programming model below, the MARC4 core has seven registers.

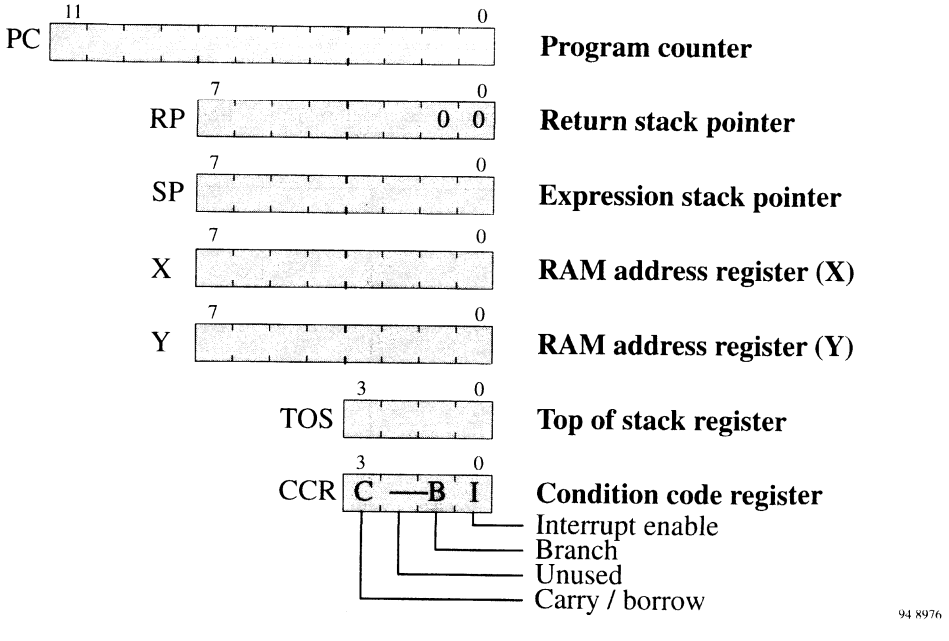


Figure 7. Programming model

2.3.1 Accumulator (TOS)

Because this microcontroller is a stack based machine with two on-chip stacks located in the internal RAM, all arithmetic , I/O and memory reference operations take their operands from, and return their results to the 4-bit wide expression stack. This stack is also used for passing parameters between subroutines, and as a scratchpad area for temporary storage of data. The top element of the expression stack is immediately accessible through the TOS register. The MARC4 can perform most of the operations dealing with the top of stack items (TOS and TOS-1) in a single byte, single cycle instruction.

2.3.2 Expression Stack Pointer (SP)

The 8-bit wide stack pointer SP contains the address of the next-to-top 4-bit item (TOS-1) on the expression stack, located in internal RAM. After power-on reset the stack pointer has to be initialised to the start address of the allocated expression stack area (S0).

2.3.3 RAM Address Register (X and Y)

The 8-bit wide register X and Y are used to address any 4-bit item in the RAM.

Using either the pre-increment address mode it is comfortable to compare, fill or move arrays in the RAM area.

2.3.4 Return Stack Pointer (RP)

The return stack pointer (RP) points to the top element of the return stack.

The 12-bit return stack is used for storing subroutine return addresses and keeping loop index counts. The return stack can also be used as a temporary storage area. The MARC4 instruction set supports the exchange of data between the top elements of the expression and return stack. The return stack automatically pre-increments and post-decrements in steps of 4. This means that every time a subroutine return address is stacked, 4-bit RAM locations are left unwritten. This locations are used by the qFORTH compiler to allocate 4-bit variables.

After power-on reset the return stack pointer has to be initialised to FCh.

2.3.5 Program Counter (PC)

The program counter (PC) is a 12-bit register that contains the address of the next instruction to be executed by the microcontroller.

2.3.6 Condition Code Register (CCR)

The 4-bit wide condition code register (CCR) indicates the results of instruction just executed as well as the state of the microcontroller. These bits can be individually tested by a program and specified action will take place as a result of their state. Each bit is explained in the following paragraphs.

Carry/Borrow (C)

This flag indicates that a borrow or carry out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during shift and rotate operations and the execution of SET_BCF, CLR_BCF and CCR! instructions.

Zero (Z)

When the bit is set, it indicates that the result of the last arithmetic or logical manipulation was zero.

Branch (B)

A conditional branch takes place when the branch flag was set by one of the previous instructions (e.g., a comparison operation).

Instructions such as SET_BCF, TOG_BF and CLR_BCF allow the direct manipulation of the branch flag under program control. The flag is affected by all ALU operations except CCR@, DI, SWI, RTI and OUT.

Interrupt enable (I)

This flag is used to interrupt processing on global basis. Resetting the interrupt enable flag (using the DI instruction) disables all interrupts. The µC does not process further interrupt requests until the interrupt enable flag is set again by either executing an EI, RTI (return-from-interrupt) instruction or entering the SLEEP mode. After power-on or an external reset the interrupt enable flag is automatically reset. The RTI instruction at the end of the $RESET routine will set the interrupt enable flag and thereby enable all interrupts.

2.3.7 Self-Check

The self test capability of the MARC4 provides the possibility of checking the core, ROM, RAM, interrupt and prescaler easily. The $RESET routine (after power-on reset) allows to choose the test routine or the application program.

Note: The necessary test routine were delivered by TEMIC.

3 Reset Modes, Interrupts, Prescaler and Low Power Modes

3.1 Reset Modes

The M43C201 has two reset modes: a power-on and an oscillator watchdog reset function.

3.1.1 Power-on Reset

The power-on reset occurs when a positive transition is detected on the power supply input. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. A power-down reset occurs when a negative transition is detected on the power supply input for 5 ms or more. To improve noise immunity the power-on reset has Schmitt-trigger characteristics as shown in figure 8.

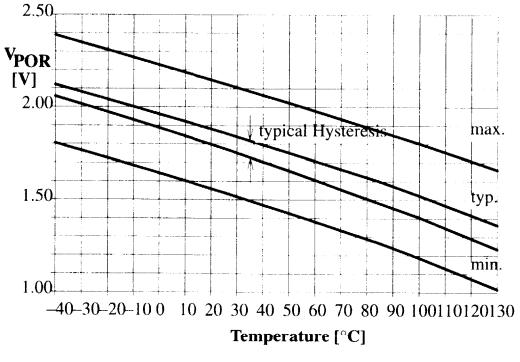


Figure 8. Temperature vs. V_{POR}

3.1.2 Oscillator – Watchdog Reset Function

The oscillator-watchdog guarantee a well-defined clock condition by using a quartz or a ceramic resonator.

After starting, normally this sorts of oscillator generates undefined clock signals. In this case the amplitude is controlled by the oscillator-watchdog. When the right value of oscillator-amplitude is detected the RST pin will be hold LOW for 32 oscillator periods. After this time the uC starts the $RESET-routine.

When extern clock is used (pin OSCOUT as clock input) the amplitude must be $0.9 \times V_{DD}$ otherwise the oscillator watchdog will detect an error.

3.1.3 Effects on Internal Circuitry

All reset modes guarantee a well-defined start condition of the complete microcontroller. During RESET all interrupts are disabled, all pending and active interrupts are cleared, all on-chip peripherals are reset and a non-maskable interrupt request is generated. The RESET has the absolute highest priority, having access to the microcontroller at all times.

	Function	Located in ROM at	Max. Length [ROM Bytes]	Interrupt Opcode
$RESET	Software & hardware initialization	008h	56	C1h

The main tasks of the reset service routine ($RESET) are:

- Stack pointer initialization,
- Variable and array initialization, and
- Initialisation and setup of the peripherals.

After execution of the reset service routine, the interrupts are enabled automatically by the RTI or previously executed EI instruction.

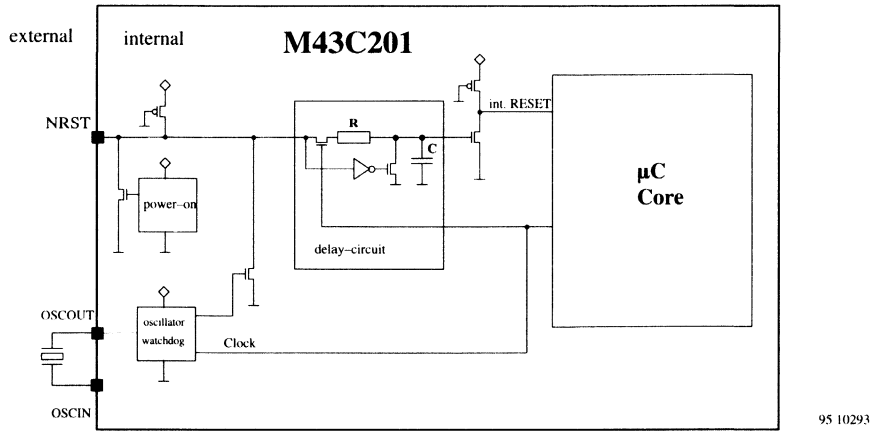


Figure 9. Reset functions

3.1.4 Summary of all Reset Functions

Figure 9 shows all reset functions: power-on and oscillator-watchdog. All these resets will generate an internal reset after passing the delay circuit. Normally the delay time is about 40 periods of the system frequency (TCL).

3.2 Interrupts

The M43C201 can handle interrupts of 8 priority levels (table 1). They are generated from on-chip modules (prescaler), external source (port 5) or synchronously from the core itself (software interrupts). Each interrupt source has a hard-wired interrupt priority and an associated interrupt service routine in the program ROM. The programmer can enable or disable all interrupts by setting or resetting the interrupt enable flag in the CCR using the EI or DI instruction.

When the interrupt enable flag is reset (interrupts disabled), the execution of interrupts is inhibited but not the logging of the interrupt requests in the interrupt pending register. While interrupts are disabled (e.g.. for a time critical section of code) and an interrupt is generated the interrupt will not be lost. Its execution will only be delayed until interrupts are enabled again. Interrupts are only lost when the pending register for a particular interrupt priority is still set at the time of a further interrupt transmission of the same level. The pending resister is reset either on power-on reset or on compilation of corresponding interrupt service routine by execution the RTI instruction (see figures 10 and 11).

The µC automatically enters the SLEEP mode when the lowest priority interrupt service routine has been completed. This guarantees a maximum use of the power saving capabilities of the µC. For further information please refer to low power modes.

Table 1. Interrupt priority and address allocation map

Priority	Function	Located in ROM at	Max. Length [ROM bytes]	Interrupt Opcode
INT7	Software interrupt	1E0h	> 24	**FCh**
INT6	Software interrupt	1C0h	32	**F8h**
INT5	Software interrupt	180h	64	**F0h**
INT4	Prescaler interrupt	140h	64	**E8h**
INT2	Software interrupt	0C0h	64	**D8h**
INT1	External hardware interrupt negative edge triggered (port 51, 52)	080h	64	**D0h**
INT0	Software interrupt	040h	64	**C8h**

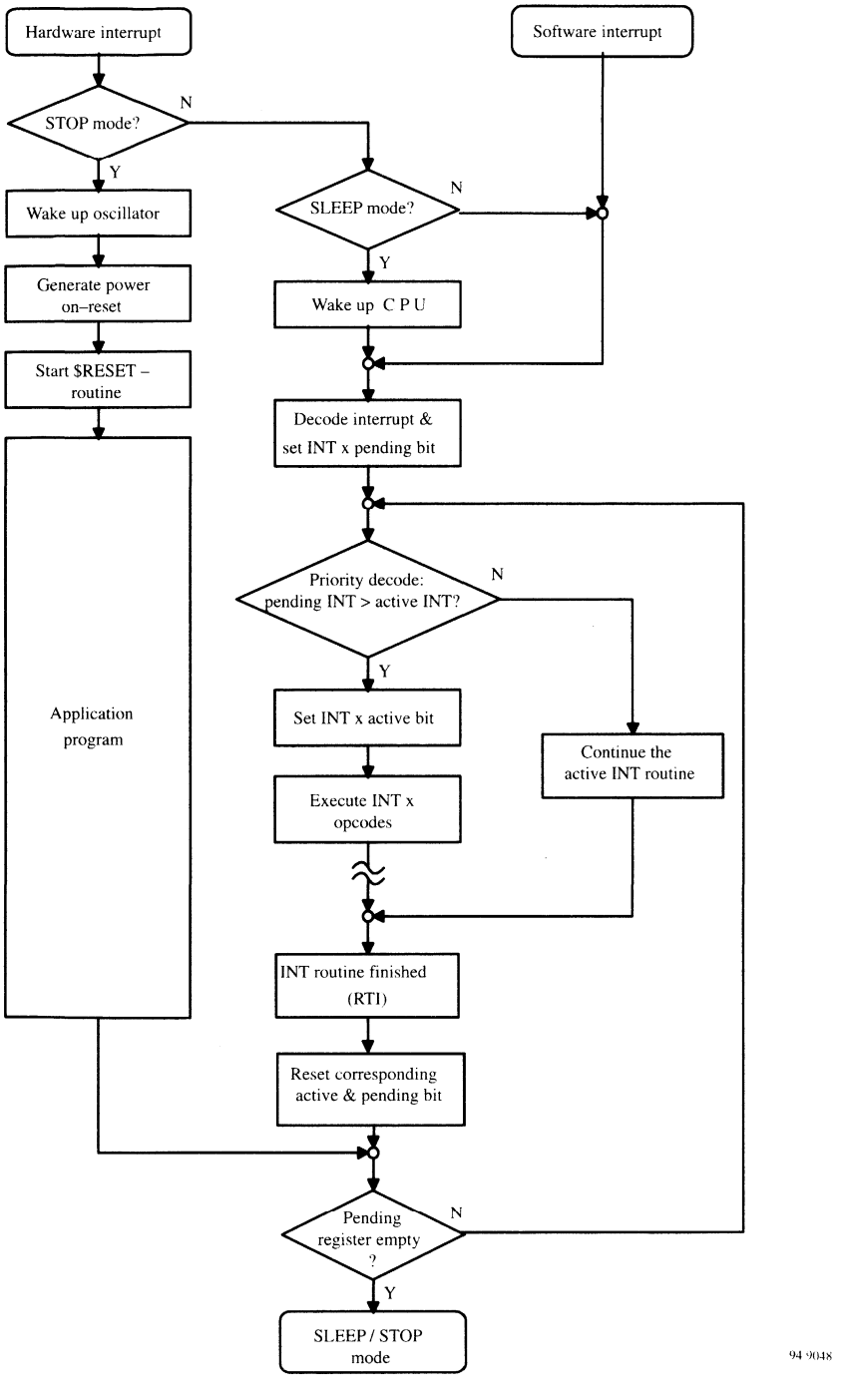


Figure 10. Interrupt flow chart

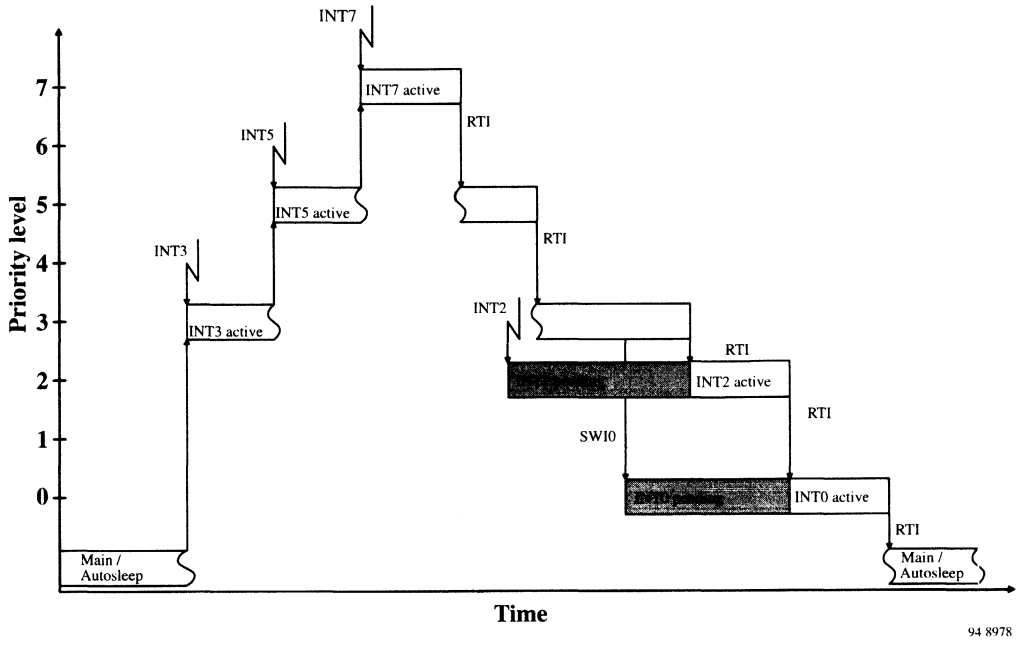


Figure 11. Interrupt processing

3.2.1 Interrupt Handling

The integrated interrupt controller samples all interrupt requests and latches these in the interrupt pending register. It also decodes the priority of the interrupt requests, and signals the µC when a higher priority interrupt requests is present. If the µC (with interrupts enabled) receives the interrupt controller's signal, an interrupt acknowledge cycle will be entered. During this cycle, the µC saves the current PC on the return stack and loads the PC with the start address of the corresponding interrupt service routine. When the µC is in the SLEEP mode, it will be activated by any hardware interrupt, by the means of wake-up the CPU and decoding the interrupt.

Using the MARC4 way of interrupt transmission, it is possible to transmit more than one interrupt at the same time. The transmitted interrupts are loaded into the interrupt pending register asynchronously. The priority decoder determines the interrupt with the highest priority and activates it as shown in figure 11. If the µC was in stop-mode any interrupt will start the oscillator. This will generate a reset and starts the $RESET routine.

3.2.2 Interrupt Latency

The interrupt latency is the time from the falling edge of the interrupt to the interrupt service routine being activated. This time is between three or five instruction cycles depending on the state of the core. The highest frequency which can be reasonably handled on the duty cycle of the application.

3.2.3 Software Interrupts

Software interrupts are executable instructions which are supported by predefined macros named SWI 0 through SWI 7. The software triggered interrupts operates exactly like any hardware triggered interrupt.

3.2.4 Hardware Interrupts

Any of the input port 51 and 52 may generate an interrupt level 1 (see figure 5). The INT1 is negative edge triggered and has Schmitt-trigger characteristics.

3.3 Prescaler Interrupt

The programmable prescaler is usually driven by an internal frequency of 31.25 kHz. The prescaler consists of a stage divider chain. This divider chain offers an interrupt source with the priority level 4. The prescaler module powers up in the reset condition which corresponds to control code Fh. The prescaler interrupt (INT4) has 15 programmable taps from 15.625 kHz down to 1 Hz. They are selectable by writing a value of E...0 into the control register at port address 15.

Table 2. Selectable interval times for the prescaler

Control Code Port Address 15	Interrupt Frequency f_C / n	f_C = 31.25 kHz Time Interval
F		reset & hold compl. presc.
E	$n = 2^1$	64 µs
D	$n = 2^2$	128 µs
C	$n = 2^3$	256 µs
B	$n = 2^4$	512 µs
A	$n = 2^5$	1.024 ms
9	$n = 2^6$	2.048 ms
8	$n = 2^7$	4.096 ms
7	$n = 2^8$	8.192 ms
6	$n = 2^9$	16.384 ms
5	$n = 2^{10}$	32.769 ms
4	$n = 2^{11}$	65.536 ms
3	$n = 2^{12}$	131.072 ms
2	$n = 2^{13}$	262.144 ms
1	$n = 2^{14}$	524.288 ms
0	$n = 2^{15}$	1.048 s

3.3.1 Prescaler during SLEEP Mode

When the microcontroller enters the SLEEP mode, the core clocks are halted. While the 4 MHz oscillator and prescaler remain active, all µC actions are suspended. The microcontroller exists in the SLEEP mode when an interrupt is generated by the prescaler (in addition to a logic low on an external interrupt (INT3), port 50, 51, 52 input pin (INT1), or an external reset).

3.4 Low Power Modes

Two low power consumption modes of operation are available: SLEEP and STOP mode. These operating modes are initiated by executing the SLEEP instruction.

Note: The SLEEP instruction is not a normal instruction as its function is depended on the state of the interrupt pending register. SLEEP is therefore available for use within the $AUTOSLEEP routine only.

3.4.1 SLEEP Mode

By executing the SLEEP instruction (in the $AUTOSLEEP routine) the microcontroller enters a low power consumption mode. In this SLEEP mode, the programmable prescaler remains active, while the internal µC-clock is turned off causing all core processing to be stopped. It can only be kept when none of the interrupt pending or active register bits are set.

During the SLEEP mode, the I bit in the condition code register (CCR) is set to enable all interrupts. All other registers, memory, and parallel input/output lines remain the same. The 4 MHz oscillator is not switched off, but the prescaler may be disabled by the application program. This mode will continue until any interrupt or reset is sensed. At this time the event is decoded and the program counter is loaded with the corresponding starting address of the interrupt or reset service routine.

The MARC4 unique AUTOSLEEP feature allows the µC to enter the SLEEP mode automatically when the lowest priority interrupt service routine has been completed.

The SLEEP mode is a shutdown condition which is used to reduce the average system power consumption in applications where the µC is not fully utilised (figure 13). Using SLEEP and interrupts, the full computational speed of the core is always available. In this way, power is only consumed when needed, allowing the µC to run in high speed bursts from a weak supply (battery, capacitor, or even a solar cell).

Calculating the average power consumption

The total power consumption is directly proportional to the active time of the µC. For a rough estimation of the expected average system current consumption, the following formula should be used:

$$I_{SYS} = I_{SLE} + (I_{DD} \times T_{active} / T_{total})$$

3.4.2 STOP Mode

The lowest power consumption mode of the microcontroller is entered with the STOP operation. The current consumption of the µC (without external loads) will be reduced to 1 µA.

The STOP mode can be implemented by switching off power supply of 4 MHz oscillator. This can be done with a combination of INRUN (BP42 = "LOW") and SLEEP.

During the STOP mode, the I bit in the CCR is set to enable external interrupts. All other registers, memory, and all I/O lines remain unchanged. This continues until an external interrupt or reset is decoded. After an external interrupt or reset the 4 MHz oscillator starts and generates a reset signal. The program counter is loaded with the reset service routine

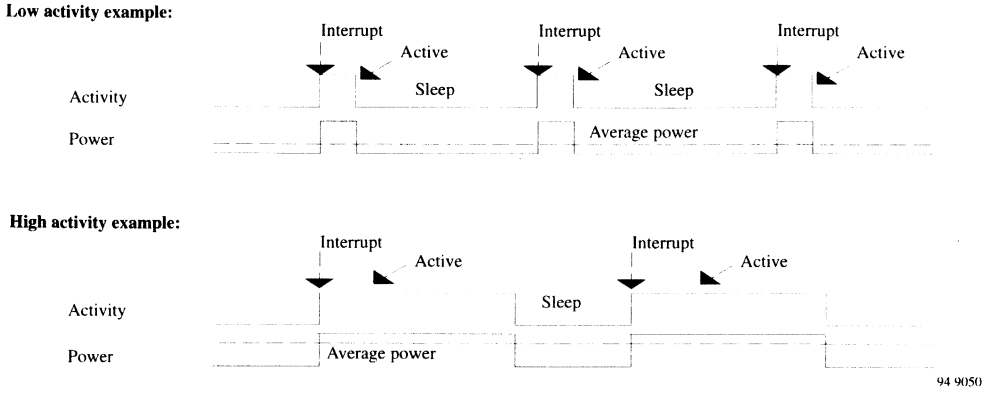


Figure 12. Average system power consumption and duty cycle

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

All voltage are given to V_{SS}. The circuit is protected against supply voltage reversal for 5 min. typ. @I_{max} = 100 mA.

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage (on any pin)	V_{IN}	V_{SS}–0.3 ≤ V_{IN} ≤ V_{DD}+0.3	V
Output short circuit duration	t_{short}	indefinite	sec
Operating temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	T_{stg}	–40 to +130	°C
Thermal resistance (PLCC)	R_{thJA}	110	K/W
Soldering temperature (t ≤ 10 sec)	T_{sd}	260	°C

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device is required. All inputs and outputs are highly protected against electrostatic discharges. However, precautions to minimize the built-up of electrostatic charges during handling.

For proper operation it is recommended that V_{IN} and V_{OUT} be limited to the range:

$$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$$

4.2 DC Operating Characteristics

Supply voltage V_{DD} = 2.4 to 6.2 V, V_{SS} = 0 V, T_{amb} = +25°C unless otherwise specified.

4.2.1 Supply Currents

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current active mode	V_{DD} = 2.4 V	I_{DD}		0.5	0.7	mA
	V_{DD} = 6.2 V			2.7	3.2	mA
Supply current SLEEP mode	V_{DD} = 2.4 V	I_{SLE}		100	130	µA
	V_{DD} = 6.2 V			600	750	µA
Supply current STOP mode	V_{DD} = 2.4 V	I_{STP}		0.08	0.1	µA
	V_{DD} = 6.2 V			0.5	0.8	µA

Input voltage pad TE, port 0, 1, 5

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Input voltage LOW	V_{DD} = 2.4 to 6.2 V	V_{IL}	V_{SS}		0.2 × V_{DD}	V
Input voltage HIGH	V_{DD} = 2.4 to 6.2 V	V_{IH}	0.8 × V_{DD}		V_{DD}	V

4.2.2 Power-on Reset (POR)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
POR voltage		V_{POR}	1.5		2.13	V
POR voltage hysteresis		ΔV_{POR}		100		mV

4.2.3 DC Electrical Characteristics, V_{DD} = 2.4 V @ 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Pad TE						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	1.1		5.0	µA
Bidirectional ports 0.0 – 0.3 and 1.0 – 1.2						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	1.1		5.0	A
Output current n-channel pull-down	$V_{OL} = V_{SS}$+0.5V	I_{OL}	0.7		2.6	mA
Output currenl p-channel pull-up	$V_{OH} = V_{DD}$–0.5V	I_{OH}	–0.6		–2.0	mA
Bidirectional port 1.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–0.8		–5.3	µA
Output current n-channel pull-down	V_{OL} = V_{SS}+0.5V	I_{OL}	0.7		2.6	mA
Output current p-channel pull-up	V_{OH} = V_{DD}–0.5V	I_{OH}	–0.6		–2.0	mA
Input port 5.1 and 5.2						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–6.1		–38.2	µA

4.2.4 DC Electrical Characteristics, V_{DD} = 6.2 V @ 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Pad TE						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	8.2		36.2	µA
Bidirectional ports 0.0 – 0.3 and 1.0 – 1.2						
Input current n-channel pull-down	$V_{IH} = V_{DD}$	I_{IH}	8.2		36.2	A
Output current n-channel pull-down	$V_{OL} = V_{SS}$ +1.3V	I_{OL}	5.0		13.0	mA
Output current p-channel pull-up	$V_{OH} = V_{DD}$–1.3V	I_{OH}	–5.0		–14.0	mA

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Bidirectional port 1.3						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–8.0		–51	µA
Output current n-channel pull-down	$V_{OL} = V_{SS} + 1.3V$	I_{OL}	5.0		13.0	mA
Output current p-channel pull-up	$V_{OH} = V_{DD} - 1.3V$	I_{OH}	–5.0		–14.0	mA
Input port 5.1 and 5.2						
Input current p-channel pull-up	$V_{IL} = V_{SS}$	I_{IL}	–58		–366	µA

4.2.5 Oscillator

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Frequency	C_L = 1 pF	f		4.0		MHz
Integrated input capacitance		C_{IN}		10		pF
Integrated output capacitance		C_{OUT}		10		pF
Start-up time quartz	V_{DD} = 2.4 V *)	t_{SQ}		8	90	ms
	V_{DD} = 3.0 V *)			4.5	10	ms
	V_{DD} = 5.0 V *)			2.5	4	ms
Start-up time ceramic	V_{DD} = 2.4 V **)	t_{SC}		250	—	µs
	V_{DD} = 3.0 V **)			150	300	µs
	V_{DD} = 5.0 V **)			150	160	µs

*) Measured with a typical quartz

C_1 = 3.2 fF
L_1 = 490 mH
R_1 = 40
C_0 = 1.4 pF

**) Ceramic

C_1 = 4.4 pF
L_1 = 385 µH
R_1 = 8.2
C_0 = 36.3 pF

4.3 I/O Port Characteristics

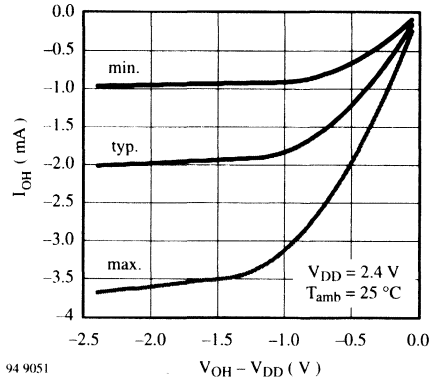


Figure 13. P-channel source current

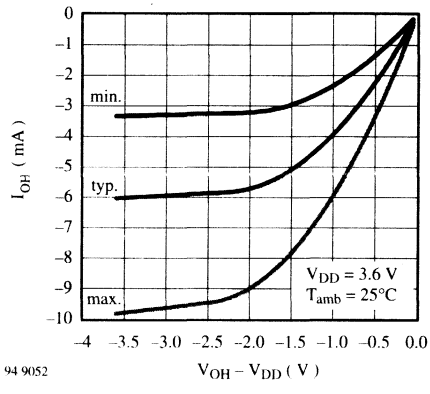


Figure 14. P-channel source current

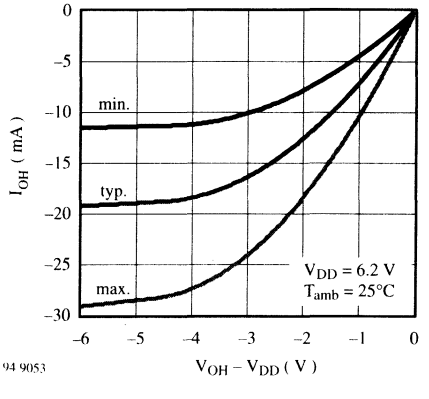


Figure 15. P-channel source current

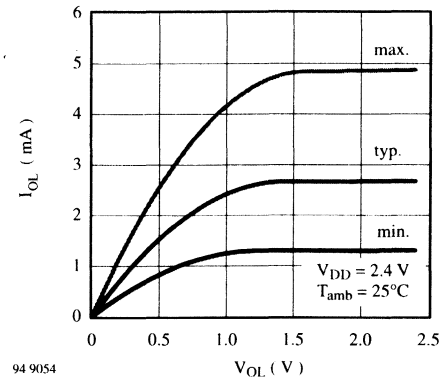


Figure 16. N-channel sink current

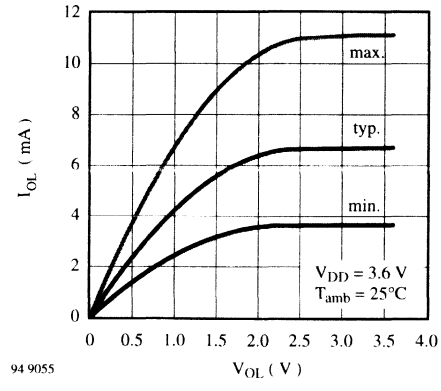


Figure 17. N-channel sink current

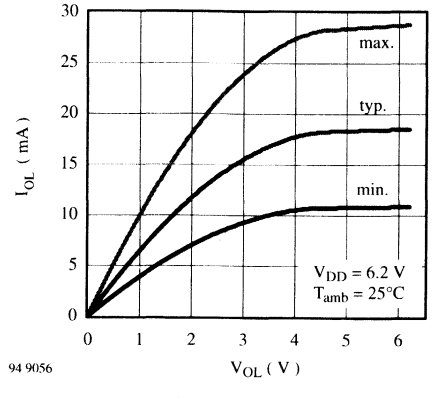


Figure 18. N-channel sink current

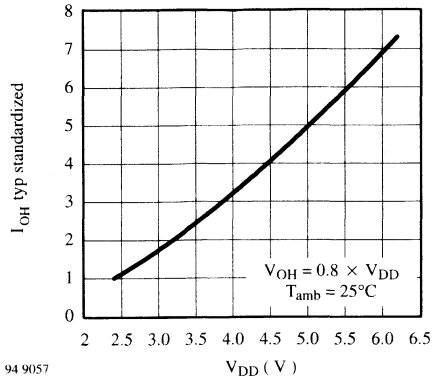


Figure 19. Standardized p-channel source vs. V_{DD}

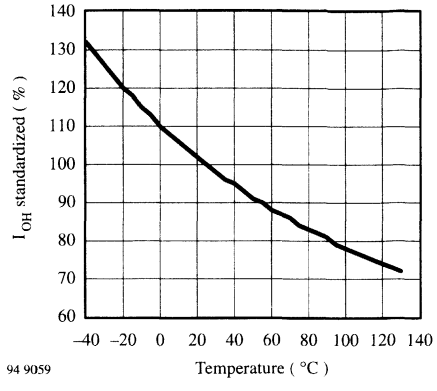


Figure 21. Standardized p-channel source current vs. ambient temperature

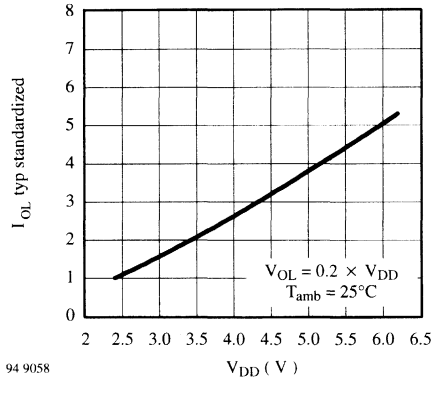


Figure 20. Standardized n-channel sink current vs. V_{DD}

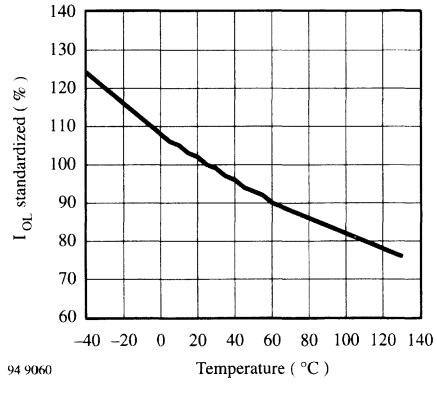


Figure 22. Standardized n-channel sink current vs. ambient temperature

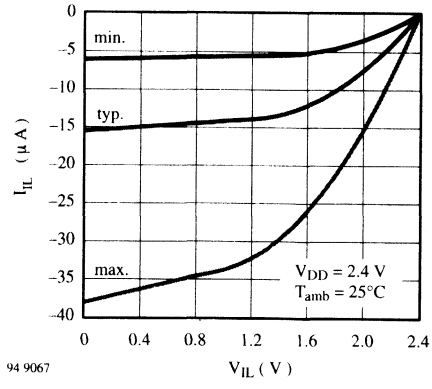


Figure 23. PIN IP5x: p-channel source current

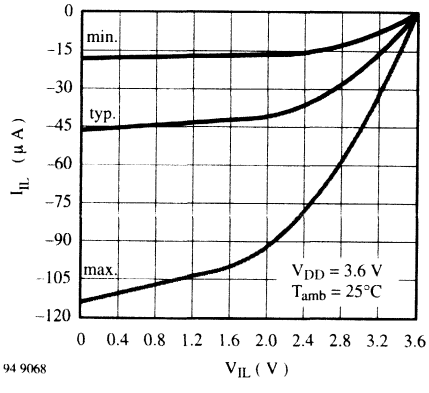


Figure 24. PIN IP5x: p-channel source current

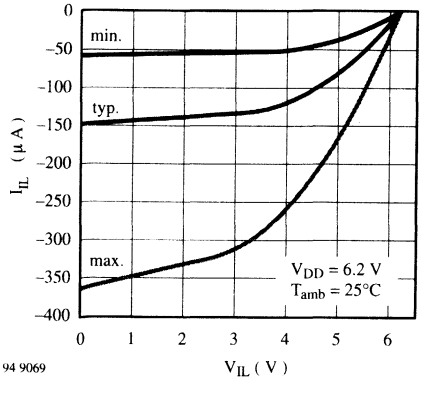


Figure 25. PIN IP5x: p-channel source current

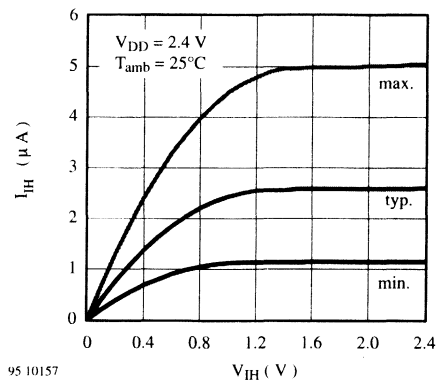


Figure 26. All PINs with pull-down: n-channel sink current

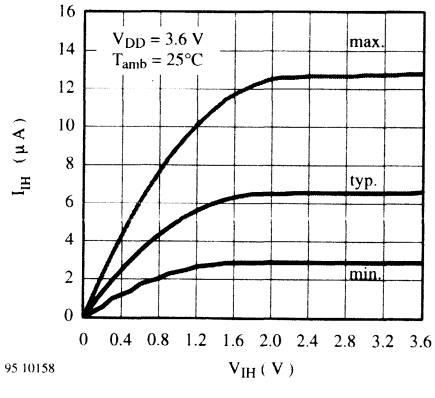


Figure 27. All PINs with pull-down: n-channel sink current

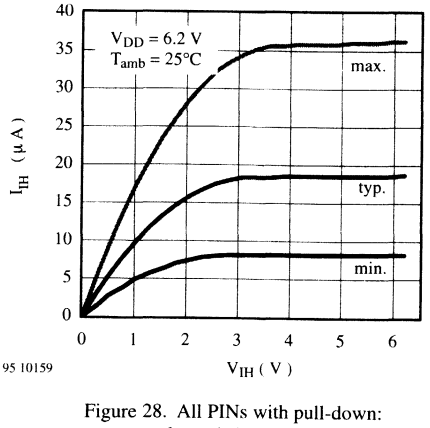


Figure 28. All PINs with pull-down: n-channel sink current

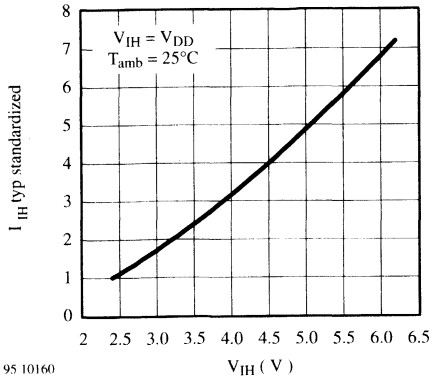


Figure 29. Standardized p-channel source current vs. V_{DD}

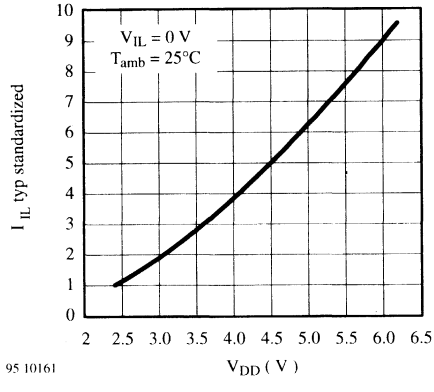


Figure 30. Standardized n-channel sink current vs. V_{DD}

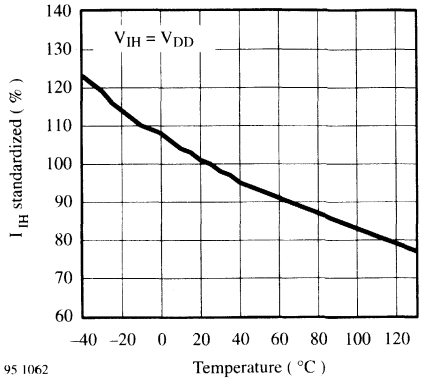


Figure 31. Standardized p-channel source current vs. ambient temperature

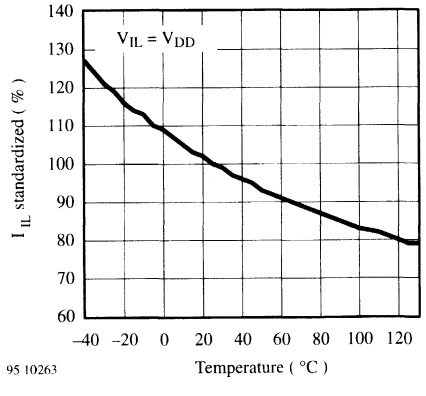
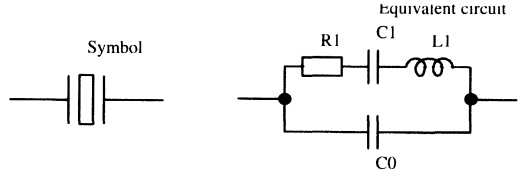


Figure 32. Standardized n-channel sink current vs. ambient temperature

5 Characteristics of the On-Chip Quartz / Ceramic Oscillator

Equivalent Circuit of the Quartz and Ceramic Resonator



The criteria for oscillation depends on R1 and C0 Following diagrams show the equivalent quartz circuits over temperature range –40 to +125°C for two different values of V_{DD}.The figure below shows the maximal values of the equivalent circuit of the ceramic-resonator which are necessary to start up by V_{DD} = 3.0 V and ambient temperature range from –40 to +125°C. For this test a resonator CSAC4.00 (MURATA) was used.

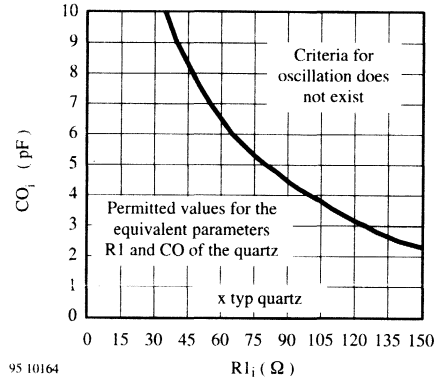


Figure 33. V_{DD} = 2.4 V

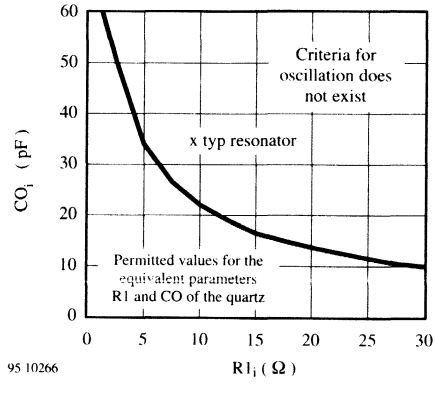


Figure 35. V_{DD} = 2.4 V

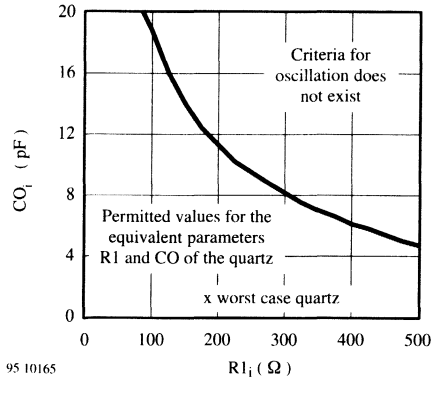


Figure 34. V_{DD} = 3.0 V

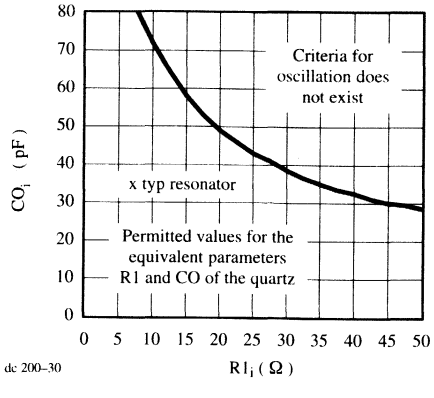


Figure 36. V_{DD} = 3.0 V

Note: For pc-board design place the quartz or ceramic resonator nearby the pins. It makes you sure that the parasitic capacities are low (≤ 0.5 pF).

6 Characteristics of the Schmitt-Trigger Inputs

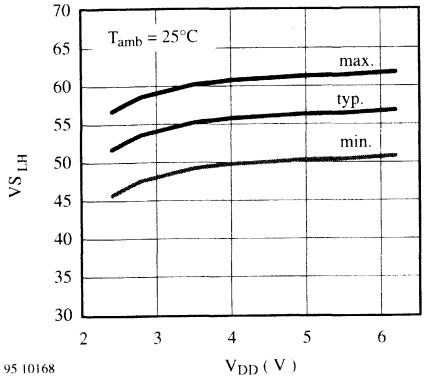


Figure 37. Voltage switch level for positive edge trigger vs. V_{DD}

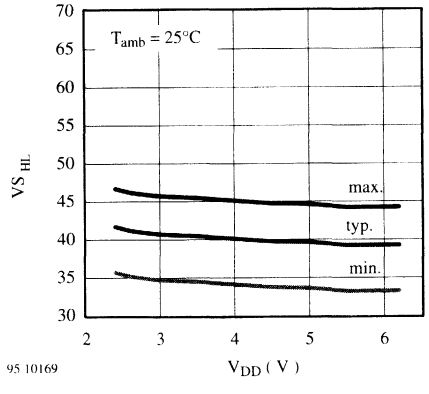


Figure 38. Voltage switch level for negative edge trigger vs. V_{DD}.

Note: The values of min., typ. and max. for the positive or negative edge trigger are matched.

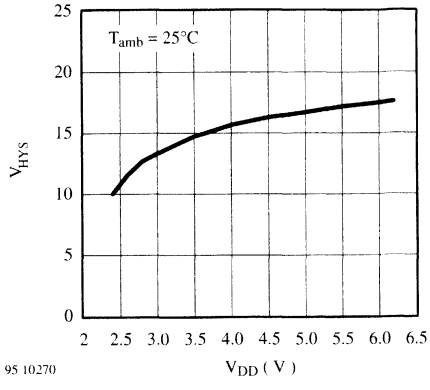


Figure 39. Hystereses in percent of supply voltage vs. V_{DD}

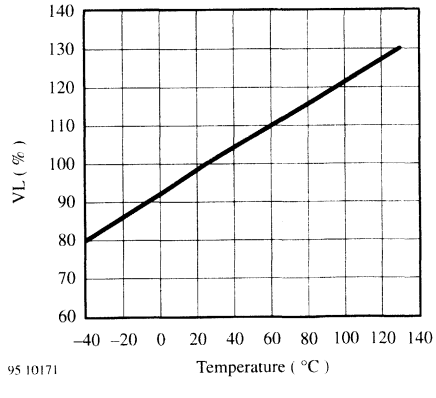


Figure 40. Typical switch level vs. ambient temperature

Note: For recognize a input pulse a minimum pulse time of 50 ns is necessary. The transition time must be ≤ 10 ns.

7 Ordering Information

Pin options

Please select the option setting from the list below.

Pin	Output		Input	
	CMOS	Open Drain	Pull-Up	Pull-Down
BP00				
BP01				
BP02				
BP03				
BP10				
BP11				
BP12				
BP13				
BP20				
BP21				
BP22				
BP23				
BP30				
BP31				
BP32				
BP33				
IP40–INT6				
IP41–TA				
IP42–TB				
IP43				
NWP				
TE				

ROM code

Please insert ROM CRC.

Size: _____ KByte **CRC:** _____ hex

Approval

Date: _____ Signature: _____

M44C260

MARC4 – 4-bit Microcontroller

The M44C260 is a member of the TEMIC family of 4-bit single chip microcontrollers. It contains ROM, RAM, EEPROM, parallel I/O ports, 1 timer with watchdog function, 2 × 8/16-bit multifunction timer/counter and the on-chip clock generation.

Features

- 4-bit HARVARD architecture
- 1 µs instruction cycle
- 4K × 8-bit application ROM
- 256 × 4-bit RAM
- 16 × 8-bit EEPROM
- 16 bidirectional I/O's
- 8 hard and software interrupt levels
- 2 × 8-bit multifunction timer/counter
- Interval timer with watchdog
- 32 kHz on-chip oscillator

Benefits

- Low power consumption
- Power down mode < 1 µA
- 2.4 to 6.2 V supply voltage
- Self test functions
- High level programming language in qFORTH

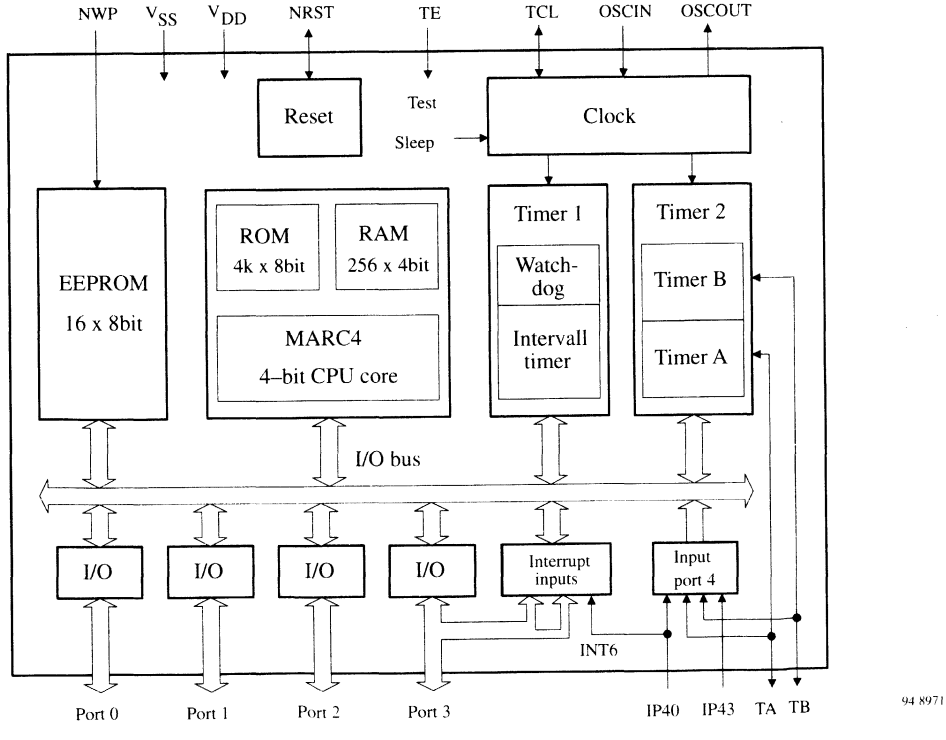


Figure 1. Block diagram

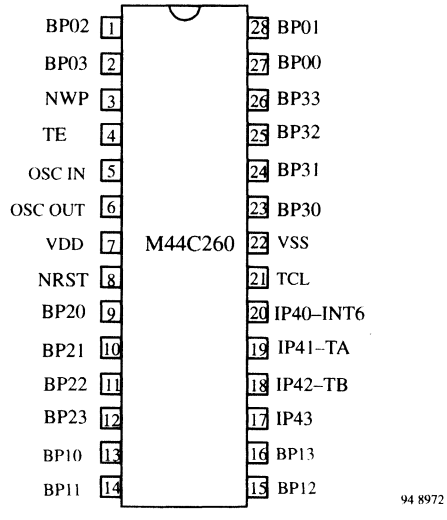


Figure 2. Pin connections

Table 1. Pin description

Name	Function
V_{DD}	Power supply voltage +2.4 to +6.2 V
V_{SS}	Circuit ground
BP00 – BP03	4 bidirectional I/O lines of port 0 *
BP10 – BP13	4 bidirectional I/O lines of port 1 *
BP20 – BP23	4 bidirectional I/O lines of port 2 *
BP30 – BP33	4 bidirectional I/O lines of port 3 with alternate interrupt function. A negative transition on BP30/BP31 requests an INT2-, and on BP32/BP33 an INT3-interrupt if the corresponding interrupt-mask is set.
IP40-INT6	Input port 40 line/interrupt 6 input * A negative transition on this input requests an INT6 interrupt if the IM6 mask bit is set.
IP41-TA	Timer/counter I/O/Input port 41 line * This line can be used as programmable I/O of counter A or as port 41 input.
IP42-TB	Timer/counter I/O/input port 42 line * This line can be used as programmable I/O of counter B or as port 42 input.
IP43	Input port 43 line *)
NWP	EEPROM write protect input, a logic low on this input protects EEPROM rows 12 to 15.
OSCIN	Oscillator input (32-kHz crystal).
OSCOUT	Oscillator output (32-kHz crystal).
NRST	Reset input/output, a logic low on this pin resets the device. An internal watchdog reset is indicated by a low level on this pin.
TCL	External system clock I/O. This pin can be used as input to provide the C with an external clock or as output of the internal system clock.
TE	Testmode input. This input is used to control the test modes and the function of the TCL pin.

*) The I/O ports have CMOS output buffers. As input they are available with pull-up or pull-down resistors. Please see the order information.

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1 MARC4 Architecture

1.1 General Description

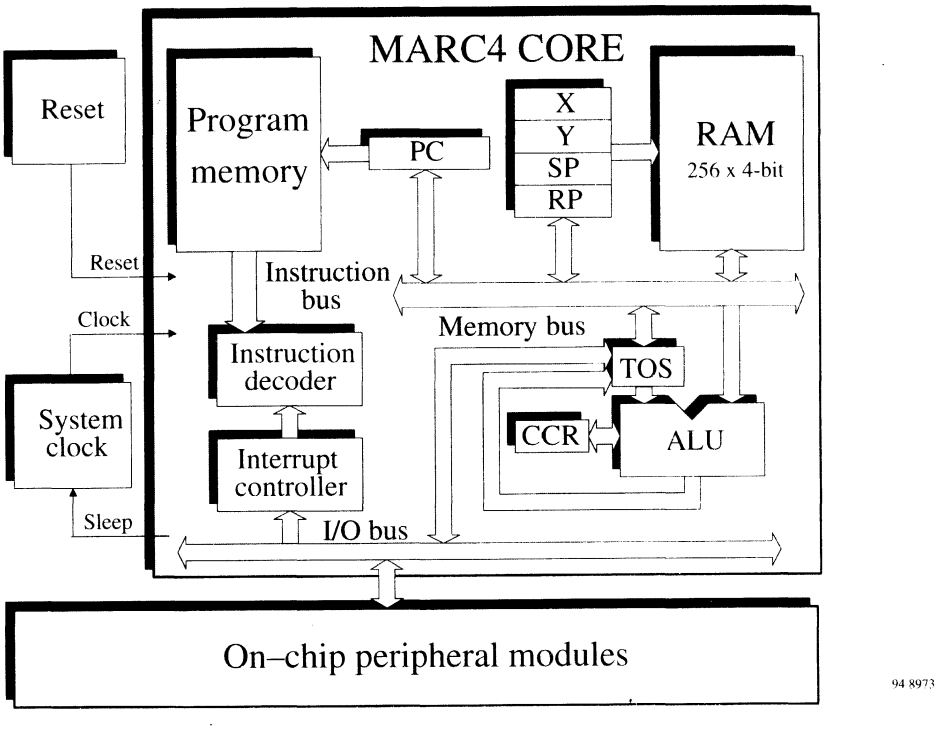


Figure 3. MARC4 core

The MARC4 microcontroller consists of an advanced stack based 4-bit CPU core and on-chip peripherals. The CPU is based on the HARVARD architecture with physically separate program memory (ROM) and data memory (RAM). Three independent buses, the instruction bus, the memory bus and the I/O bus are used for parallel communication between ROM, RAM and peripherals. This enhances program execution speed by allowing both instruction prefetching, and a simultaneous communication to the on-chip peripheral circuitry. The integrated powerful interrupt controller with eight prioritized interrupt levels, supports fast processing of hardware events.

The MARC4 is designed for the high level programming language qFORTH. The core contains both FORTH stacks, expression stack and return stack. This architecture allows high level language programming without any loss in efficiency or code density.

1.2 Components of MARC4 Core

The core contains ROM, RAM, ALU, program counter, RAM address register, instruction decoder and interrupt controller. The following sections describe each of this parts.

1.2.1 Program Memory (ROM)

The program memory (ROM) is mask programmed with the customer application program during the fabrication of the microcontroller. The ROM is addressed by a 12-bit wide program counter, thus limiting the program size to a maximum of 4 Kbytes. An additional 1 Kbyte ROM is available for test software only.

The user ROM starts with a 512 byte segment (zero page) which contains predefined start addresses for interrupt service routines and special subroutines accessible with single byte instructions (SCALL). The corresponding memory map is shown in figure 4.

Look-up tables of constants can also be held in ROM and are accessed via the MARC4's built-in TABLE instruction.

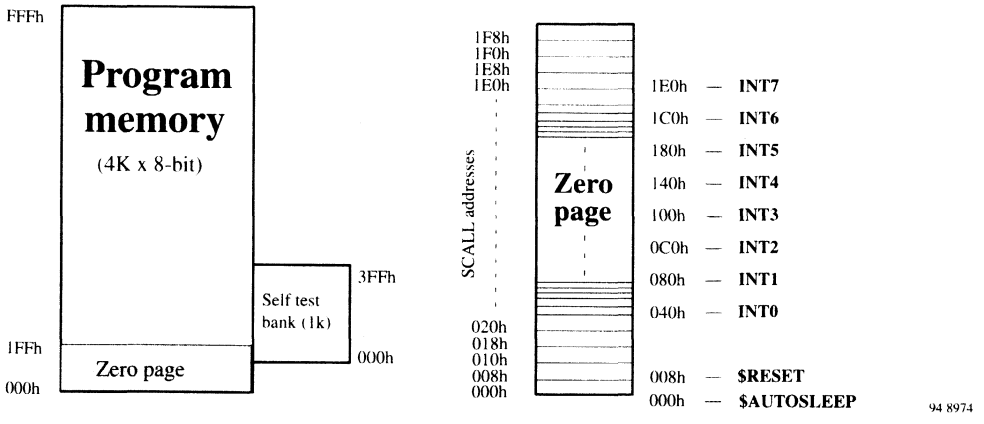


Figure 4. Progam memory map

1.2.2 Data Memory (RAM)

The MARC4 contains 256 x 4-bit wide static random access memory (RAM). It is used for the expression stack, the return stack and data memory for variables and arrays. The RAM is addressed by any of the four 8-bit wide RAM address registers SP, RP, X and Y.

- Expression Stack

The 4-bit wide expression stack is addressed with the expression stack pointer (SP). All arithmetic, I/O and memory reference operations take their operands from, and return their result to the expression stack. The MARC4 performs the operations with the top of stack items (TOS and TOS-1). The TOS register contains the top element of the expression stack and works like an accumulator. This stack is also used for passing parameters between subroutines, and as a scratchpad area for temporary storage of data.

- Return Stack

The 12-bit wide return stack is addressed by the return stack pointer (RP). It is used for storing return addresses of subroutines, interrupt routines and for keeping loop index counts. The return stack can also be used as a temporary storage area.

The MARC4 instruction set supports the exchange of data between the top elements of the expression stack and the return stack. The two stacks within the RAM have a user definable location and maximum depth.

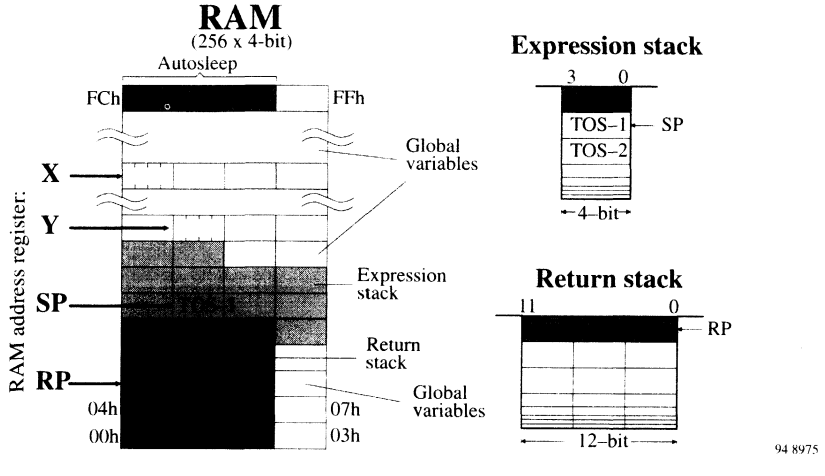


Figure 5. RAM map

1.2.3 Registers

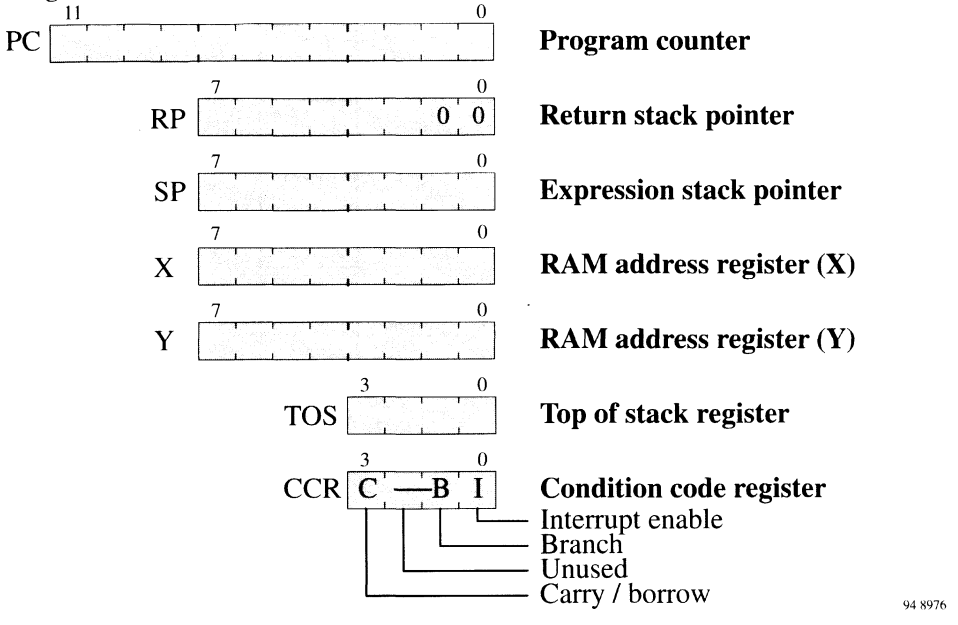


Figure 6. Programming model

The MARC4 controller has six programmable registers and one condition code register. They are shown in the following programming model.

- Program Counter (PC)

The program counter (PC) is a 12-bit register that contains the address of the next instruction to be fetched from the program memory. Instructions currently being executed are decoded in the instruction decoder to determine the internal micro operations. For linear code (no calls or branches) the program counter is incremented with every instruction cycle. If a branch-, call-, return-instruction or an interrupt is executed the program counter is loaded with a new address. The program counter is also used with the TABLE instruction to fetch 8-bit wide ROM constants.

RAM address register

The RAM is addressed with the four 8-bit wide RAM address registers: SP, RP, X and Y. These registers allow access to any of the 256 RAM nibbles.

- Expression Stack Pointer (SP)

The stack pointer (SP) contains the address of the next-to-top 4-bit item (TOS-1) of the expression stack. The pointer is automatically pre-incremented if a nibble is moved onto the stack or post-decremented if a nibble is removed from the stack. Every post-decrement operation moves the item (TOS-1) to the TOS register before the SP is decremented. After a reset the stack pointer has to be initialized with " >SP $xx " to allocate the start address of the expression stack area.

- Return Stack Pointer (RP)

The return stack pointer points to the top element of the 12-bit wide return stack. The pointer automatically pre-increments if an element is moved onto the stack or it post-decrements if an element is removed from the stack. The return stack pointer increments and decrements in steps of 4. This means that every time a 12-bit element is stacked, a 4-bit RAM location are left unwritten. These location are used by the qFORTH compiler to allocate 4-bit variables. After a reset the return stack pointer has to be initialized with " >RP FCh ".

- RAM Address Register (X and Y)

The X and Y registers are used to address any 4-bit item in the RAM. A fetch operation moves the addressed nibble onto the TOS. A store operation moves the TOS to the addressed RAM location. Using either the pre-increment or post-decrement addressing mode arrays in the RAM can be compared, filled or moved.

- Top Of Stack (TOS)

The top of stack register is the accumulator of the MARC4. All arithmetic/logic, memory reference and I/O operations use this register. The TOS register gets the data from the ALU, the program memory, the RAM or via the I/O bus.

- Condition Code Register (CCR)

The 4-bit wide condition code register contains the branch, the carry and the interrupt enable flag. These bits indicates the current state of the CPU. The CCR flags are set or reset by ALU operations. The instructions SET_BCF, TOG_BF, CCR! and DI allow a direct manipulation of the condition code register.

Carry/Borrow (C)

The carry/borrow flag indicates that borrow or carry out of arithmetic logic unit (ALU) occurred during the last arithmetic operation. During shift and rotate operations this bit is used as a fifth bit. Boolean operations have no affect on the C flag.

Branch (B)

The branch flag controls the conditional program branching. When the branch flag was set by one of the previous instructions a conditional branch is taken. This flag is affected by arithmetic, logic, shift, and rotate operations.

Interrupt Enable (I)

The interrupt enable flag enables or disables the interrupt processing on a global basis. After reset or by executing the DI instruction the interrupt enable flag is reset and all interrupts are disabled. The µC does not process further interrupt requests until the interrupt enable flag is set again by either executing an EI, RTI or SLEEP instruction.

1.2.4 ALU

The 4-bit ALU performs all the arithmetic, logical, shift and rotate operations with the top two elements of the expression stack (TOS and TOS-1) and returns its result to the TOS. The ALU operations affect the carry/borrow and branch flag in the condition code register (CCR).

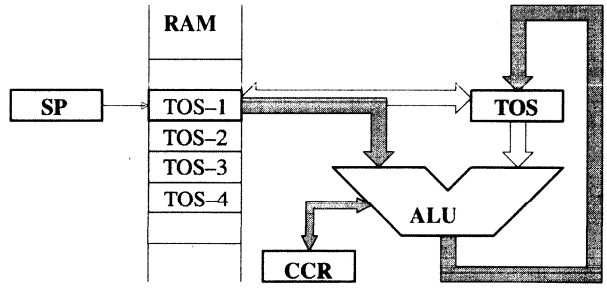


Figure 7. ALU zero address operations

1.2.5 Instruction Cycles

A MARC4 instruction word is one or two byte long and is executed within one or four machine-cycles. A machine–cycle consists of two system clocks (SYSCL). The MARC4 is a zero address machine. Most of the instructions are one byte long and are executed in only one machine–cycle. The CPU has an instruction pipeline, this allows the controller to fetch the next instruction from program memory at the same time as the present instruction is being executed. For more informations see section "MARC4 Instruction Set Overview".

1.2.6 I/O Bus

The I/O ports and the registers of the peripheral modules (timer 1, timer 2, EEPROM) are I/O mapped. The communication between the core and the on-chip peripherals takes place via the I/O bus and the associated I/O control bus. These buses are used for different functions: for read and write accesses, for the interrupt generation, to reset peripherals and for the SLEEP mode. With the MARC4 IN-instruction and OUT-instructions the I/O bus allows a direct read or write access to one of the 16 I/O addresses. More about the I/O access to the on-chip peripherals is described in the section "Peripheral modules".

The I/O buses are internal buses and are not accessible by the customer on the final microcontroller device, but they are used as the interface for the MARC4 emulation (see also the section "Emulation").

1.2.7 Interrupt Structure

The MARC4 can handle interrupts with eight different priority levels. They can be generated from the internal and external interrupt sources or by a software interrupt from the CPU itself. Each interrupt level has a hard-wired priority and an associated vector for the service routine in the ROM (see table 2). The programmer can enable or disable interrupts all together by setting or resetting the interrupt enable flag (I) in the CCR.

Interrupt processing

For processing the eight interrupt levels the MARC4 contains an interrupt controller with the 8-bit wide interrupt pending and interrupt active register. The interrupt controller samples all interrupt requests during every non-I/O instruction cycle and latches them in the interrupt pending register. If no higher priority interrupt is present in the interrupt active register it signals the CPU to interrupt the current program execution. If the interrupt enable bit is set the processor enters an interrupt acknowledge cycle. During this cycle a SHORT CALL instruction to the service routine is executed and the current PC is saved on the return stack. An interrupt service routine is finished with the RTI instruction. This instruction sets the interrupt enable flag, resets the corresponding bits in the interrupt pending/active register and fetches the return address from the return stack to the program counter. When the interrupt enable flag is reset (interrupts are disabled), the execution of interrupts is inhibited but not the logging of the interrupt requests in the interrupt pending register. The execution of the interrupt will be delayed until the interrupt enable flag is set again. But note that interrupts are lost if an interrupt request occurs during the corresponding bit in the pending register is still set. After the reset (power-on, external or watchdog reset), the interrupt enable flag and the interrupt pending and interrupt active register are reset.

Interrupt latency

The interrupt latency is the time from the falling edge of the interrupt to the interrupt service routine being activated. In the MARC4 this takes between 3 to 5 machine cycles depending on the state of the core.

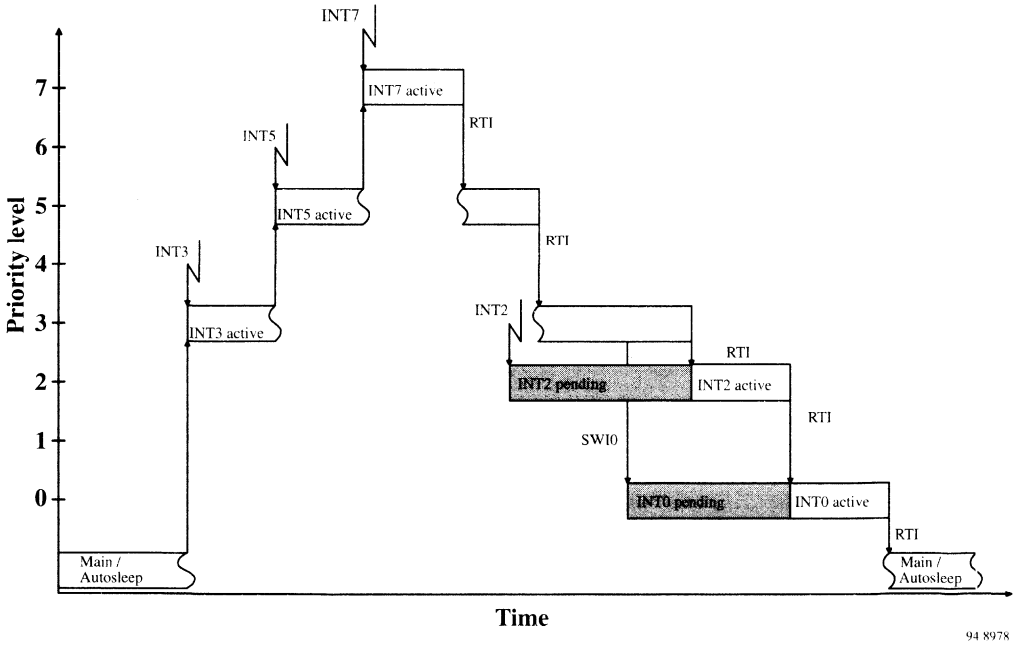


Figure 8. Interrupt handling

Table 2. Interrupt priority table

Interrupt	Priority	Vector Address	Interrupt Opcode (Acknowledge)	Function
INT0	lowest	040h	C8h (SCALL 040h)	Software interrupt (SWI0)
INT1		080h	D0h (SCALL 080h)	EEPROM write ready
INT2		0C0h	D8h (SCALL 0C0h)	External hardware interrupt, neg. edge at BP30 or BP31
INT3		100h	E0h (SCALL 100h)	External hardware interrupt, neg. edge at BP32 or BP33
INT4		140h	E8h (SCALL 140h)	Timer 1 interrupt
INT5		180h	F0h (SCALL 180h)	Timer 2 interrupt
INT6		1C0h	F8h (SCALL 1C0h)	External hardware interrupt, neg. edge at IP40 pin
INT7	highest	1E0h	FCh (SCALL 1E0h)	Software interrupt (SWI7)

Software Interrupts

The programmer can generate interrupts using the software interrupt instruction (SWI) which is supported in qFORTH by predefined macros named SWI0 to SWI7. The software triggered interrupt operates exactly like any hardware triggered interrupt. The SWI instruction takes the top two elements from the expression stack and writes the corresponding bits via the I/O bus to the interrupt pending register. Thus using the SWI instruction, interrupts can be re-prioritized or lower priority processes scheduled for later execution.

Hardware Interrupts

In the M44C260 are eleven hardware interrupt sources with six different levels. Each of these sources can be enabled or disabled separately with an interrupt mask bit in the IMR1 or IMR2 register.

Table 3. Hardware interrupts

Interrupt	Priority	Mask		Interrupt Source
		Register	Bit	
EEPROM write ready	INT1	EMS	IMEP	EEPROM end of write cycle
External interrupt port 3 (BP30 OR BP31)	INT2	IMR1	IM30	Negative edge at BP30
			IM31	Negative edge at BP31
External interrupt port 3 (BP32 OR BP33)	INT3	IMR1	IM32	Negative edge at BP32
			IM33	Negative edge at BP33
Timer 1 interrupt	INT4	IMR2	IMT1	Timer 1
Timer 2 interrupt	INT5	T2IC	IMAS	Timer A end of space/underflow
			IMAP	Timer A end of pulse/capture
			IMBS	Timer B end of space/underflow
			IMBP	Timer B end of pulse/capture
Ext. interrupt IP40 input	INT6	IMR2	IM6	Negative edge at IP40 input

1.3 Reset

The reset puts the CPU into a well-defined condition. The reset can be triggered by switching on the supply voltage, by a break-down of the supply voltage, by the watchdog timer or by pulling the NRST pad to low.

After any reset the branch-, carry- and interrupt enable flag in the Condition Code Register (CCR) , the interrupt pending register and the interrupt active register are reset.

During the reset-cycle the I/O bus control signals are set to 'reset mode' thereby initializing all on-chip peripherals.

A reset is finished with a short call instruction (opcode C1h) to the program memory address 008h. This activates the initialization routine $RESET. With that routine the stack pointers, variables in the RAM and the peripheral must be initialized.

Power-on Reset

The power-on reset ensures that the core is activated not before the operating supply voltage has been reached.

A reset is also generated when the supply voltage remains below the operating range for more than 5 ms.

External Reset (NRST)

An external reset can be triggered with the NRST pin. For the external reset the pin should be low for a minimum of two machine cycles.

Watchdog Timer Reset

If the watchdog timer function of Timer 1 is enabled a reset is triggered with every watchdog counter overflow. To suppress that the watchdog counter must be reset by an access to the CWD-register (see also Timer 1/watchdog counter).

The power-on reset and watchdog reset are indicated in the same way as an external reset on the NRST pad.

1.4 Clock Generation

The M44C260 has two oscillators, one RC oscillator for the system clock generation and an additional 32-kHz crystal oscillator. The system clock generator provides the core and Timer 2 with the clock. The system clock frequency of the M44C260 is programmable for 1 or 2 MHz. The crystal oscillator is used as an exact time base for Timer 1. If no exact timing is required, the controller does not need an external crystal. In this case Timer 1 is provided with the system clock.

The configuration for both oscillators is programmable with the clock status control register (CSC), which is a subport register located in port CSUB. The required configuration has to be initialized after reset in the $RESET routine. The default setting after a reset is 1 MHz system clock and an active 32-kHz crystal oscillator.

After power-on or a SLEEP instruction the clock generator needs a start-up time until it runs with an exact timing. The CRDY bit in the CSC register indicates the start-up phase.

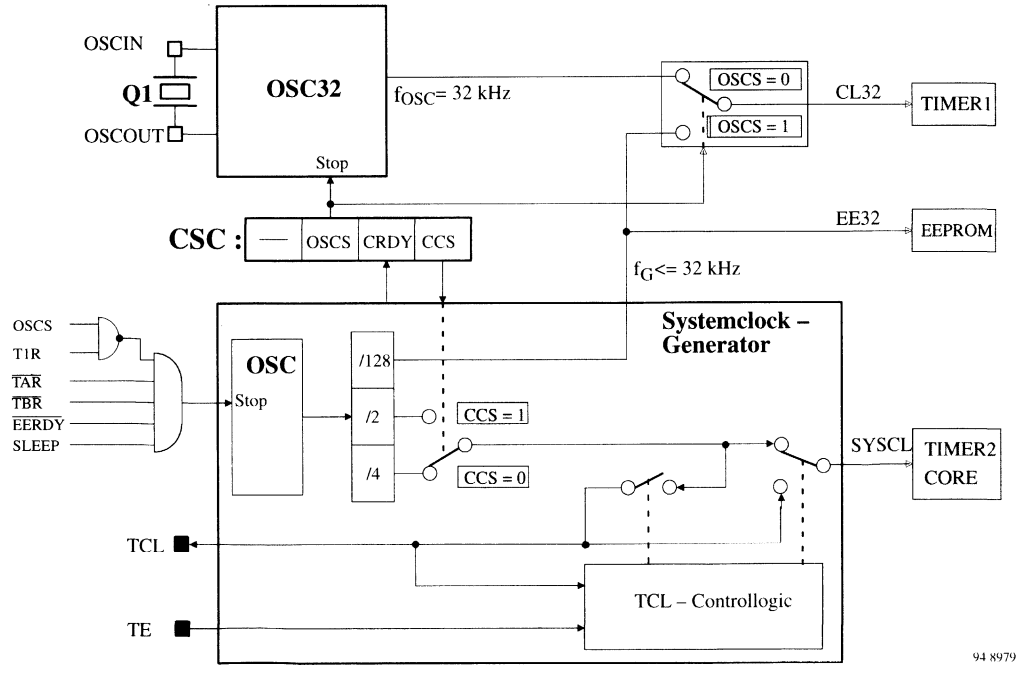


Figure 9. Clock module

1.4.1 Clock Status/Control Register (CSC)

Address: Ch Subaddress: 2h

	Bit 3	Bit 2	Bit 1	Bit 0	
CSC	—	OSCS	CRDY	CCS	**Reset value: X000h**

OSCS **Oscillator Stop**
When OSCS = 0 the controller is configured to run with the 32-kHz crystal oscillator for Timer 1.
When OSCS = 1 the 32-kHz oscillator stops. For µC operation without crystal, this bit must be set after reset. In that case Timer 1 is provided from the internal RC oscillator.

CRDY **Clock Ready (status bit)**
CRDY = 0 indicates the start-up time of the oscillators.
CRDY = 1 indicates that the clock is ready. The µC runs with an exact timing.

CCS **Core Clock Select**
CCS = 0 selects 1 MHz system clock (SYSCL/TCL)
CCS = 1 selects 2 MHz system clock (SYSCL/TCL)

1.4.2 TCL Signal

The TCL pin can be used as input to supply the controller with an external clock. For this configuration the TCL pin must be held low for at least 0.5 ms during the reset cycle. The controller is working with clock frequencies up to 2.5 MHz. It is also possible to use the TCL pin as output to supply peripherals with the system clock. In this case the TE pin must be connected to V_{DD} level and the TCL pin must have a high impedance load.

1.5 Power Down Modes

The sleep mode is a shutdown condition which is used to reduce the average system power consumption in applications where the µC is not fully utilized. In this mode the system clock is stopped. The sleep mode is entered with the SLEEP instruction. This instruction sets the interrupt enable bit (I) in the condition code register to enable all interrupts and stops the core. During the sleep mode the peripheral modules remain active and are able to generate interrupts. The µC exits the sleep mode with any interrupt or a reset.

The sleep mode can only be kept when none of the interrupt pending or active register bits are set. The application of the $AUTOSLEEP routine ensures the correct function of the sleep mode.

The total power consumption is directly proportional to the active time of the µC. For a rough estimation of the expected average system current consumption, the following formula should be used:

$$I_{total}\,(V_{DD}, f_{Osc}) = I_{Sleep} + (I_{DD} * T_{active}/T_{total})$$

I_{DD} depends on V_{DD} and f_{Osc}.

Systemclock Generator Stop

The M44C260 has different power down modes. When the MARC4 core enters the sleep mode and no on-chip peripheral needs a clock signal (SYSCL) the system clock oscillator is stopped. Therefor the programmer should stop timer 1 and timer 2 during the sleep mode if they are not required. If the 32-kHz oscillator is not used it should be stopped. Under this condition the power consumption is extremely low (see following table).

Table 4. Power consumption at different power down modes

Mode	CPU-Core	TIMER 1 [T1R] TIMER 2 [TAR, TBR] EEPROM [EERDY]	RC Osc.	32-kHz-Osc. [OSCS]	Power-Consumption [µA]
1	SLEEP	T1R=0 AND TAR=0 AND TBR=0 AND EERDY=1	STOP	STOP	< 1.0
2	SLEEP	T1R=X, TAR=0 AND TBR=0 AND EERDY=1	STOP	RUN	< 1.0
3	SLEEP	T1R=1 OR TAR=1 OR TBR=1 OR EERDY=0	RUN	STOP	< x
4	SLEEP	T1R=X, TAR=1 OR TBR=1 OR EERDY=0	RUN	RUN	< x
5	RUN	T1R=X, TAR=X, TBR=X, EERDY=X	RUN	STOP	< y
6	RUN	T1R=X, TAR=X, TBR=X, EERDY=X	RUN	RUN	< y

2 Peripheral Modules

2.1 Addressing Peripherals

The access to the peripheral modules (ports, registers) is executed via the I/O bus. The IN- or OUT-instruction allows the direct addressing of 16 I/O ports. For the peripherals with a large number of registers, extended addressing is used. With two I/O operations an extended I/O port allows the access to 16 subports. The first OUT-instruction writes the subport address to the subaddress register, the second IN- or OUT-instruction reads data from or writes data to the addressed subport.

Table 5. I/O-addressing

I/O Operation	qFORTH Instructions	Description
Port 0, 1, 2, 3, 4, T2SC, EMS		
I/O read	port IN	Read data from port
I/O write	data port OUT	Write data to port
T2SUB, CSUB		
Extended I/O read	subaddress port OUT	Write subaddress to port
	port IN	Read data from subaddress
Extended I/O write	subaddress port OUT	Write subaddress to port
	data port OUT	Write data to subaddress
Extended I/O short read	port IN	Read data from current subaddress
ESUB		
Extended I/O read (byte)	subaddress port OUT	Write subaddress to port
	port IN	Read data high nibble from subaddress
	port IN	Read data low nibble from subaddress
Extended I/O write (byte)	subaddress port OUT	Write subaddress to port
	data port OUT	Write data low nibble to subaddress
	data port OUT	Write data high nibble to subaddress

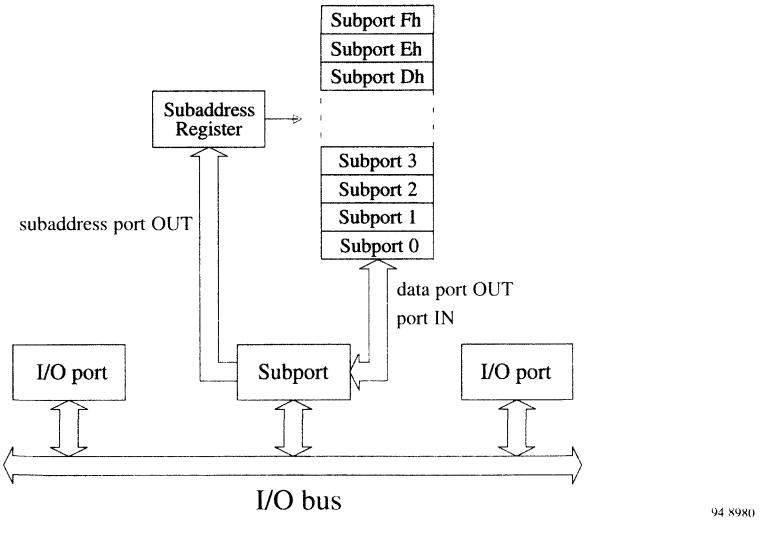


Figure 10. Extended I/O addressing

Table 6. Peripheral addresses

Addr.	Name	Function			
0	Port 0	Bidirectional port			
1	Port 1	Bidirectional port			
2	Port 2	Bidirectional port			
3	Port 3	Bidirectional port			
4	Port 4	Input port			
5	—				
6	—				
7	—				
8	T2SC	Timer 2 status and control register			
9	T2SUB	Subport for timer 2	Sub-address	Name	Register
			0	TARCH	Timer 2A space reload/capture register, high nibble
			1	TARCL	Timer 2A space reload/capture register, low nibble
			2	TARH	Timer 2A pulse reload register
			3	TARL	Timer 2A pulse reload register
			4	TBRCH	Timer 2B space reload/capture register, high nibble
			5	TBRCL	Timer 2B space reload/capture register, low nibble
			6	TBRH	Timer 2B pulse reload register
			7	TBRL	Timer 2B pulse reload register
			8	TAM1	Timer 2A mode register 1
			9	TAM2	Timer 2A mode register 2
			A	TBM1	Timer 2B mode register 1
			B	TBM2	Timer 2B mode register 2
			C	T2IC	Timer 2 interrupt control
			D	T2PC	Timer 2 prescaler control
			E	—	
			F	—	
A	EMS	EEPROM status register			
B	ESUB	Subport for EEPROM	Row 0 – Row F		
C	CSUB	Subport for watchdog, timer 1, interrupt masks, and clock generator	Sub-address	Name	Register
			0	WDC	Watchdog control register
			1	CWD	Clear watchdog counter
			2	CSC	Clock status/control register
			3	—	
			4	T1C	Timer 1 control register
			5	IMR1	Interrupt mask register 1
			6	IMR2	Interrupt mask register 2
			7-F	—	
D	—				
E	—				
F	—				

2.1.1 Input Port 4

Port 4 is the input port for the pins IP40, IP43, TA and TB. IP40 is also the interrupt input for INT6, and TA and TB are normally used for timer I/O functions.

	Bit 3	Bit 2	Bit 1	Bit 0
Input port 4	**IP43**	**TB/IP42**	**TA/IP41**	**IP40/INT6**

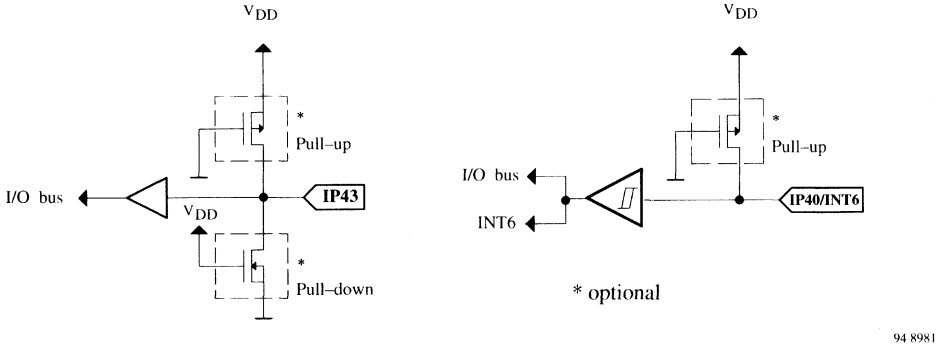


Figure 11. Input port IP40, IP43

2.1.2 Bidirectional Ports

Ports 0, 1, 2 and 3 are bidirectional 4-bit wide ports and may be used for data input or output. The data direction is programmable for a complete port only. The port is switched to output with an OUT-instruction and to input with an IN-instruction. The data written to a port will be stored into the output latches and appears immediately after the OUT-instruction at the port pin. After RESET all output latches are set to Fh and the ports are switched to input mode.

Note: Care must be taken when switching bidirectional ports from output to input. The capacitive load at this port may cause the data read to be the same as the last data written to this port. To avoid this, when switching the direction one of the following approaches should be used.

- Use two IN-instructions and DROP the first data nibble read. The first IN switches the port from output to input, DROP removes the first invalid nibble and the second IN reads the valid nibble.
- Use an OUT-instruction followed by an IN-instruction. With the OUT-instruction the capacitive load is charged or discharged depending on the optional pull-up /pull-down configuration. Write a "1" for pins with pull-up resistors and a "0" for pins with pull-down resistors.

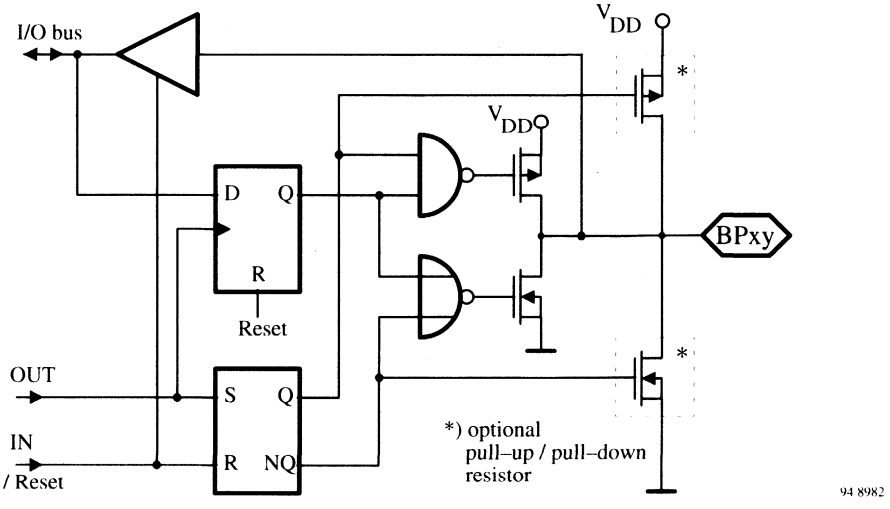


Figure 12. Bidirectional port

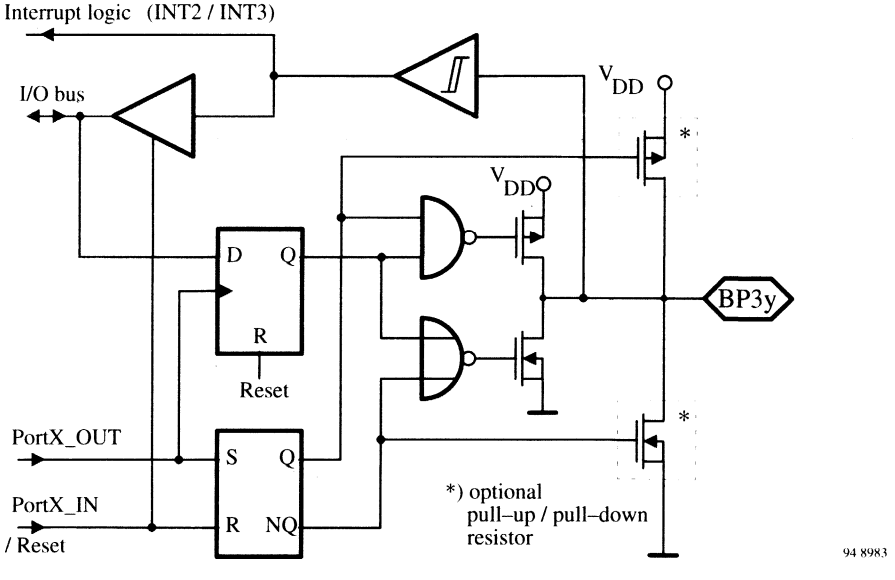


Figure 13. Bidirectional port 3 with interrupt input

2.1.3 External Interrupt Inputs

The pins IP40 and BP30 – BP33 can be used as external interrupt inputs. IP40 is used for INT6, BP32 and BP33 are used for INT3, and BP30 and BP31 are used for INT2. Pin IP40 is also used as an input port and BP30 – BP33 as a bidirectional port (see figure 11). Each of these external interrupt sources can be enabled or disabled with individually interrupt mask bits. A negative transition at one of these inputs requests an interrupt, when the corresponding mask bit is set. The interrupt masks are placed in the subport registers IMR1 and IMR2 of port CSUB.

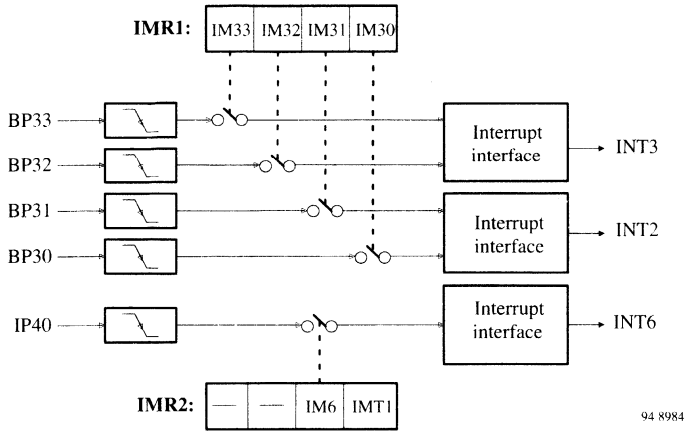


Figure 14. External interrupt inputs

2.2 Timer 1

Timer 1 is an interval timer for generating interrupts. Additional to the timer can be used as watchdog timer. The timer consists of a programmable 18 stage divider which is supplied with a 32-kHz clock and a 3-bit counter for the watchdog function (see figure 15). The time interval for a timer 1 interrupt (INT4) can be programmed with the timer control register from 1 ms up to 8.0 s. The timer 1 interrupt is maskable with the IMT1 bit.

The time interval for a watchdog reset can be programmed with the watchdog control register for 0.5, 2.0, 8.0 or 16.0 s. When the watchdog is active (WDR = 1, T1R = 1) the controller is reset with the overflow of the 3-bit watchdog counter. The application software has to ensure that the watchdog counter is reset by a write access to the CWD port before it overflows. Because the watchdog timer is supplied by the interval timer it is necessary that timer 1 is set active (T1R = 1).

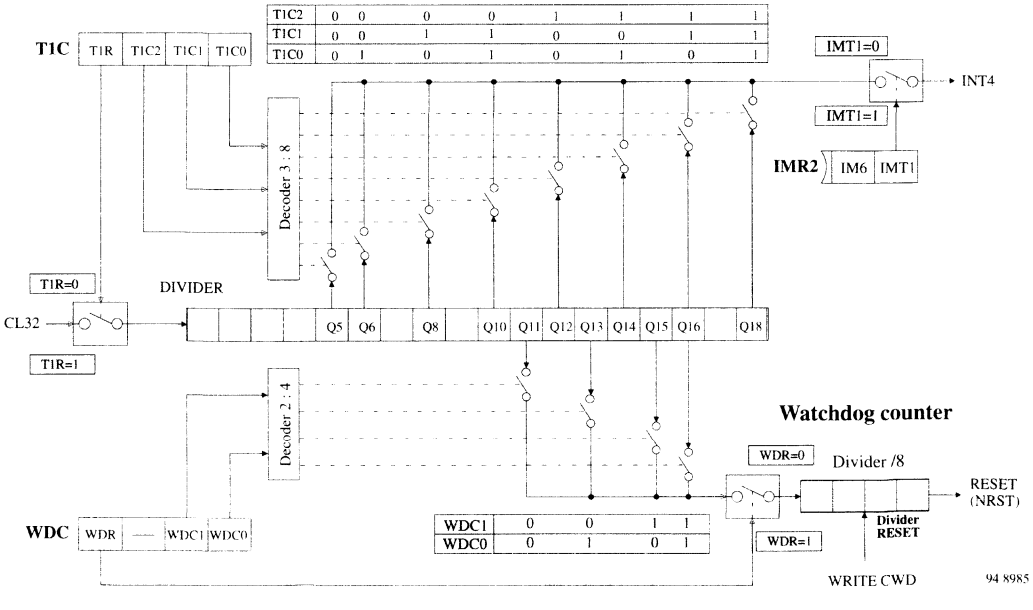


Figure 15. Timer 1

Timer 1 register

The registers of Timer 1 are I/O-mapped. They are sub-port register of port CSUB the access is made by extended I/O operations. The interval timer is controlled by the prescaler control register T1C. The interrupt mask IMT1 is placed in the interrupt mask register IMR2. The watch-dog timer is controlled by the watchdog control register WDC and port CWD. A write access to CWD resets the watchdog counter.

2.2.1 T1C – Timer 1 Control Register

Address: 'C'h Subaddress 4

	Bit 3	2	1	0
T1C	**T1R**	**T1C2**	**T1C1**	**T1C0**

Reset value: 0000b

T1R Timer 1 run
T1R = 0 stops the interval timer
T1R = 1 starts the interval timer

T1C2 Timer 1 control bit 2

T1C1 Timer 1 control bit 1

T1C0 Timer 1 control bit 0

This both bits select the time interval for a Timer 1 interrupt.

T1C2	T1C1	T1C0	Divider	Time Interval
0	0	0	32	0.9765625 ms
0	0	1	64	1.953125 ms
0	1	0	256	7.8125 ms
0	1	1	1024	31.25 ms
1	0	0	4096	125 ms
1	0	1	16384	500 ms
1	1	0	65536	2 s
1	1	1	262144	8 s

2.2.2 WDC – Watchdog Control Register

Address: 'C'h Subaddress 0

	Bit 3	2	1	0
WDC	**WDR**	—	**WDM1**	**WDM0**

Reset value: 0x00b

WDR Watchdog run
WDR = 0 the watchdog counter is inactive and reset
WDR = 1 the watchdog counter is active and able to generate a reset when Timer 1 is running

WDC1 Watchdog mode 1

WDC0 Watchdog mode 0

This both bits control the time interval for the watchdog reset.

WDM 1	WDM 0	Divider	Delay time to Reset (s)
0	0	2048	0.5
0	1	8192	2
1	0	32768	8
1	1	524288	16

2.3 Timer 2

Timer 2 consists of the two timer/counter blocks Timer A and Timer B. Each block has one 8-bit downcounter and a programmable prescaler. The clock inputs can be programmed to count the system clocks, Timer A clocks or external clocks. The maximum clock rate for external clocks is the half system clock frequency (SYSCL/2). Each counter has a reload register for the pulse time and a reload register for the space time. Every counter underflow toggles the output and reloads the downcounter alternately from the pulse reload register or from the space reload register. This allows the generation of any duty cycles.

Addition both counters have a capture mode. In this mode an external signal or the Counter B output causes the current counter value to be captured into the corresponding capture register.

The timer has two I/O pins, TA for Timer A and TB for Timer B. Used as output the pins have a high level during the pulse time and a low level during the space time of the timer. As input the pins are used for the external counter clock or the capture signal. The inputs have a programmable edge detection to select the active edge of an external clock or capture signal.

Interrupts can be generated when a counter underflow or a capture event occurs. The interrupt function for timer 2 can be programmed with the interrupt control register. Both counter blocks share one interrupt vector (INT5).

Timer 2 Modes

There are various timer/counter modes for both blocks of Timer 2. They can be used separately or combined. The timer modes can be programmed with the timer control and mode registers.

Single Timer Modes

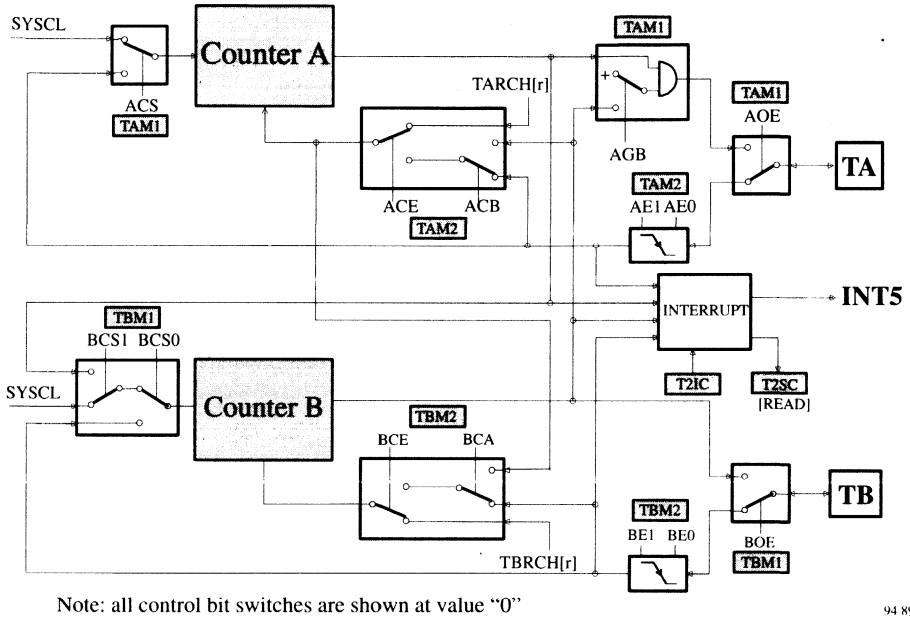
- **8-bit timer**
  Counter A/B is supplied by the system clock and is used to generate timer interrupts.
- **Pulse width modulation**
  Counter A/B is supplied by the system clock. The TA/TB pin is used as counter output. The duty cycle can be programmed with the pulse and space reload register.
- **Capture mode**
  Counter A/B is supplied by the system clock. The TA/TB pin is used as input. An external signal at the input causes the current counter value to be captured into the capture register.
- **Event counter**
  Counter A/B counts external clocks at the TA/TB pin. The capture register contains the current counter value and can be read.

Combined Timer Modes

- **16-bit timer**
  Counter A is supplied system clock and its output is coupled with the input of Counter B. In this mode the counter is used to generate timer interrupts.
- **16 bit capture mode**
  Counter A is supplied with the system clock and Counter B with the output of Counter A. An external signal at the TA pin causes the current counter value will be captured into the capture registers.
- **16-bit event counter**
  The output of Counter A is coupled with the input of Counter B to count external clocks at TA. The capture register of both counters contain the current counter values.
- **Burst generator**
  Counter A is supplied the system clock and its output is coupled with the input of Counter B. The output of Counter B controls the output signal of Counter A at the TA pin. The TA output is enabled during the pulse and disabled during the space of Counter B.
- **Event counter with time gate**
  Counter A counts the clocks at the TA pin and Counter B is supplied with the system clock. Each underflow of Counter B causes the counter value of Counter A to be captured into its capture register.

Timer 2 Register

All timer register are I/O mapped. The access to the Timer 2 status control register (T2SC) can be done with a direct I/O operation to T2SC. The status is read with an IN operation and a command to control the timer is written with an OUT operation. The remaining registers of Timer 2 are subport registers of port T2SUB. The access to those registers needs an extended I/O operation. The timer function can be configured with the mode registers TAM1, TAM2, TBM1, TBM2 and the interrupt control register T2IC. The timing depends on the contents of the prescaler control register T2PC and the reload registers. The capture registers are used to read the counter value.



Note: all control bit switches are shown at value "0"

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Figure 16. Timer 2

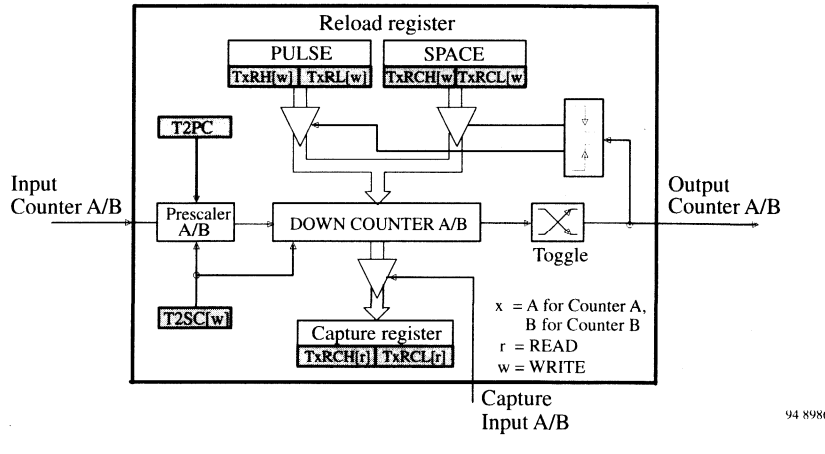

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Figure 17. Counter A/B

2.3.1 Timer 2 Status/Control Register (T2SC)

Address: 8

	Bit 3	2	1	0	
Control register **Write (T2SC)**	**TBM**	**TAM**	**TBR**	**TAR**	**Reset value: 0000b**
Status register **Read (T2SC)**	**TBSU**	**TBPC**	**TASU**	**TAPC**	**Reset value: 0000b**

TAM, TAR: Timer A control bits to start or stop Timer A.

TBM, TBR: Timer B control bits to start or stop Timer B.

TBM	TAM	TBR	TAR	Timer 2 Commands
1	0	x	0	STOP_A
1	0	x	1	RUN_A
0	1	0	x	STOP_B
0	1	1	x	RUN_B
0	0	0	0	STOP_AB
0	0	1	1	RUN_AB
0	0	0	1	RUN_A-STOP_B
0	0	1	0	STOP_A-RUN_B
1	1	x	x	NOP

A STOP command resets the prescaler and counter.

A RUN command starts the counter with the next clock taking the value from the pulse reload register.

TBSU: Timer B end of space/underflow status bit.
When BCE* = 0 this bit will be set at the end of space time of Counter B.
When BCE = 1 this bit will be set with every Counter B underflow.

TBPC: Timer B end of pulse/capture status bit.
When BCE = 0 this bit will be set at the end of pulse time of Counter B.
When BCE = 1 this bit will be set when a capture event for Counter B occurs.

TASU: Timer A end of space/underflow status bit.
When ACE* = 0 this bit will be set at the end of space time of Counter A.
When ACE = 1 this bit will be set with each Counter A underflow.

TAPC: Timer A end of pulse/capture status bit.
When ACE = 0 this bit will be set at the end of pulse time of Counter A.
When ACE = 1 this bit will be set when a capture event for Counter A occurs.

*) ACE and BCE are the capture enable control bits in the timer mode registers TAM2 and TBM2.

The status bits TASU, TAPC, TBSU, TBPC will be reset after a READ access to T2SC!

2.3.2 Timer 2 Subport (T2SUB)

Address: 9

Table 7. Timer 2 subports

Subaddr.	Name	Meaning	Bit 3	Bit 2	Bit 1	Bit 0
0	TARCH [w]*	Timer A reload high	High-nibble			
	TARCH [r]*	Timer A capture high				
1	TARCL [w]*	Timer A reload low	Low-nibble			
	TARCL [r]*	Timer A capture low				
2	TARH	Timer A reload high	High-nibble			
3	TARL	Timer A reload low	Low-nibble			
4	TBRCH [w]*	Timer B reload high	High-nibble			
	TBRCH [r]*	Timer B capture high				
5	TBRCL [w]*	Timer B reload low	Low-nibble			
	TBRCL [r]*	Timer B capture low				
6	TBRH	Timer B reload high	High-nibble			
7	TBRL	Timer B reload low	Low-nibble			
8	TAM1	Timer A mode register 1	—	AGB	ACS	AOE
9	TAM2	Timer A mode register 2	ACB	ACE	AE1	AE0
A	TBM1	Timer B mode register 1	—	BCS1	BCS0	BOE
B	TBM2	Timer B mode register 2	BCA	BCE	BE1	BE0
C	T2IC	Timer 2 interrupt control	IMBS	IMBP	IMAS	IMAP
D	T2PC	Timer 2 prescaler control	BPC1	BPC0	APC1	APC0
E	—		—	—	—	—
F	—		—	—	—	—

* [w] write only, [r] read only

2.3.3 Timer 2 Reload Register

The 8–bit wide reload registers of Timer A and B are used to program the pulse and space width of the counter output signal.

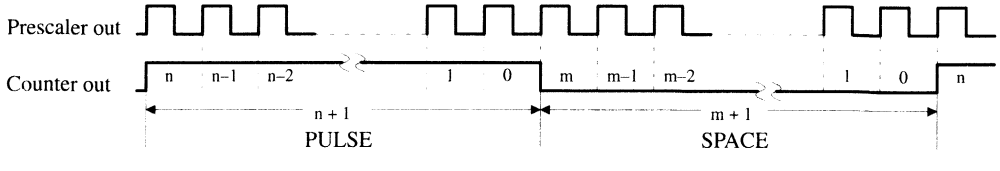
The first clock after a start command loads the downcounter with the value (n) from the pulse reload register and sets the counter output to 1. The downcounter decrements with each following clock and each underflow reloads alternately the value (m) from the space reload register or the value (n) from the pulse reload register and toggles the counter output.

The pulse and space width can be calculated as following:

Pulse time: Pulse = (n+1) x prescaler clocks

Spacetime: Space = (m+1) x prescaler clocks

$$0 \leq m, n \leq 255$$



Timer 2 Space Reload Register

The space reload register of Timer 2 is programmed by two write accesses to the subport addresses TARCH and TARCL or TBRCH and TBRCL of the Timer 2 subport T2SUB. The value (m) in the space reload register determines the space width. At the end of pulse the downcounter reloads the 8–bit value from the space reload register with the next clock of the prescaler output.

Space width: Space = (m+1) prescaler clocks

$0 \leq m \leq 255$

Timer 2 Pulse Reload Register

The pulse reload register of Timer 2 is programmed by two write accesses to the subport addresses TERH and TARL or TBRH and TBRL of the Timer 2 subport T2SUB. The value (n) in the pulse reload register determines the space width. At the end of space the downcounter reloads the 8–bit value from the pulse reload register with the next clock of the prescaler output.

Pulse width: Pulse = (n+1) prescaler clocks

$0 \leq n \leq 255$

2.3.4 Timer 2 Capture Register

The capture register is used to capture the current downcounter value when a capture event occurs. The value is kept in the capture register until the next capture event and can be read independent of the state of the downcounter. The capture events are programmable with the timer mode registers TAM2 and TBM2.

The capture registers are also used to read the counter value when the external capture mode is disabled. In this case the 8–bit counter value is transferred into the capture register by reading the high nibble TARCH or TBRCH. If the 16–bit event counter mode is enabled the complete 16–bit value is captured by reading first the high nibble TARCH of Timer A. This mechanism ensures the coherence of the counter high and low nibble during the read access.

2.3.5 Timer A Mode Register 1 (TAM1)

Address: 9 – Subaddress: 8

	Bit 3	2	1	0
TAM1	—	**AGB**	**ACS**	**AOE**

Reset value: 0000b

AGB Counter **A** output gated by Counter **B** output
AGB = 1 enables the burst generation mode. The output of Timer A is enabled during the pulse time of the Counter B and disabled (TA= 0) during the space time of the Counter B.

ACS Counter **A** clock select
This bit selects the source of the Counter A clock. When ACS = 0 the timer is supplied with internal SYSCL. When ACS = 1 the timer is supplied with an external clock on TA pin.

AOE Timer **A** output enable
AOE = 0 disables the counter output TA.
AOE = 1 enables the counter output TA.

2.3.6 Timer A Mode Register 2 (TAM2)

Address: 9 – Subaddress: 9

	Bit 3	2	1	0
TAM2	**ACB**	**ACE**	**AE1**	**AE0**

Reset Value: 0000b

ACB Timer **A** captured by Timer **B**
Selects the capture source for Timer A. When ACB = 0 the signal at the TA pin is used to generate a capture event. When ACB = 1 each transition at the Counter B output is used to generate a capture event for Timer A.

ACE Timer **A** capture enable
ACE = 1 enables the capture mode for Counter A. The occurrence of a capture event causes that the current downcounter value is loaded into the capture register.

AE1 Timer **A** edge select bit **1**

AE0 Timer **A** edge select bit **0**
Whit these bits the active edge for the counter clocks and capture signal is selected.

AE1	AE0	Active Edge for Counter Clock/Capture Events
0	0	positive edge at TA pin
0	1	negative edge at TA pin
1	0	first positive edge after timer start and then each transition at TA pin
1	1	first negative edge after timer start and then each transition at TA pin

2.3.7 Timer B Mode Register 1 (TBM1)

Address: 9 – Subaddress: Ah

	Bit 3	2	1	0
TBM1	**—**	**BCS1**	**BCS0**	**BOE**

Reset value: 0000b

BCS1 Timer **B** clock select bit **1**

BCS0 Timer **B** clock select bit **0**

These bits select the source of Counter B clock.

BCS1	BCS0	Counter B Input Signal
0	0	System clock (SYSCL)
1	0	Output signal of Counter A
x	1	External input signal at TB

BOE Timer **B** output enable
BOE = 0 disables the counter output TB.
BOE = 1 enables the counter output TB.

2.3.8 Timer B Mode Register 2 (TBM2)

Address: 9 – Subaddress: Bh

	Bit 3	2	1	0
TBM2	**BCA**	**BCE**	**BE1**	**BE0**

Reset value: 0000b

BCA Timer B is captured with Timer A capture signal. With BCA = 1 the external capture signal for Timer A is used to capture Timer B
simultaneously with Timer A.
Note: It is possible to capture Counter B by a read access to TARCH

BCE Timer **B** capture enable
BCE = 1 enables the capture mode for Counter B. A capture event loads the current downcounter value into the capture register.

BE1 Timer **B** edge select bit **1**

BE0 Timer **A** edge select bit **0**
With these bits the active edge for the counter clocks and capture signal is selected.

BE1	BE0	Active Edge for Clock/Capture Events
0	0	positive edge on TB pin
0	1	negative edge on TB pin
1	0	first positive edge after start timer and then each transition on TB pin
1	1	first negative edge after start timer and then each transition on TB pin

2.3.9 Timer 2 Prescaler Control Register (T2PC)

Address: 9 – Subaddress: Dh

	Bit 3	2	1	0
T2PC	**BPC1**	**BPC0**	**APC1**	**APC0**

Reset Value: 0000b

BPC1 Timer **B** prescaler control bit **1**

BPC0 Timer **B** prescaler control bit **0**
These bits determine the divider for the prescaler of Timer B.

APC1 Timer **A** prescaler control bit **1**

APC0 Timer **A** prescaler control bit **0**
These bits determine the divider for the prescaler of Timer A.

BPC1/APC1	BPC0/APC0	Divider
0	0	1
0	1	4
1	0	16
1	1	64

2.3.10 Timer 2 Interrupt Control Register (T2IC)

Address: 9 – Subaddress: Ch

	Bit 3	2	1	0
T2IC	**IMBS**	**IMBP**	**IMAS**	**IMAP**

Reset value: 0000b

IMBS Interrupt mask Timer B end of space/underflow
IMBS = 1 enables an INT5 interrupt, if BCE* = 0 at the end of space of Counter B, or if BCE = 1 at each Counter B underflow.

IMBP Interrupt mask Timer B end of pulse/capture
IMBP = 1 enables an INT5 interrupt, if BCE = 0 at the end of pulse of Counter B, or if BCE = 1 with a capture event for Counter B.

IMAS Interrupt mask Timer A end of space/underflow
IMAS = 1 enables an INT5 interrupt, if ACE* = 0 at the end of space of Counter A, or if ACE = 1 at each Counter A underflow.

IMAP Interrupt mask Timer A end of pulse/capture
IMAP = 1 enables an INT5 interrupt, if ACE = 0 at the end of pulse of Counter A, or if ACE = 1 with a capture event for Counter A.

Each interrupt source can be enabled or disabled individually by setting the corresponding maskbit.

*) ACE and BCE are the capture enable control bits in the timer mode registers TAM2 and TBM2.

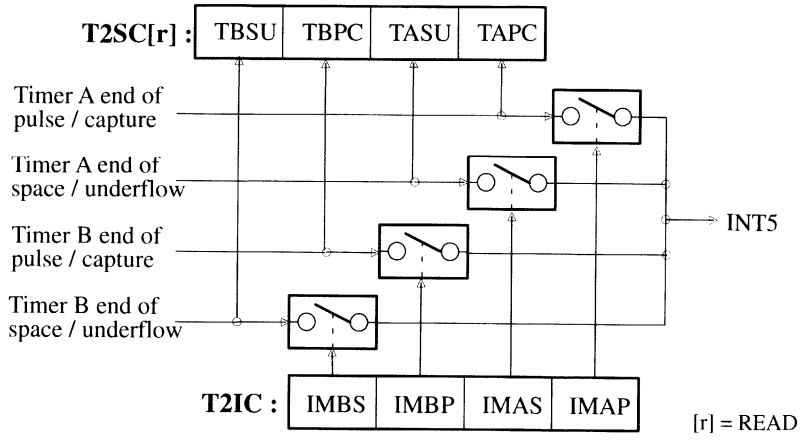


Figure 18. Timer 2 interrupt mask register

2.3.11 Timer I/O (TA/TB)

The timer I/O pins TA and TB are used as input for the external clock or capture signal and as output for the counter. The mode is controlled with AOE and BOE control bit. When AOE/BOE = 0 the pin is switched to input mode, when AOE/BOE = 1 the pin is switched to output mode. The pins also can be read with an IN-instruction via port 4 (TA with IP41 and TB with IP42).

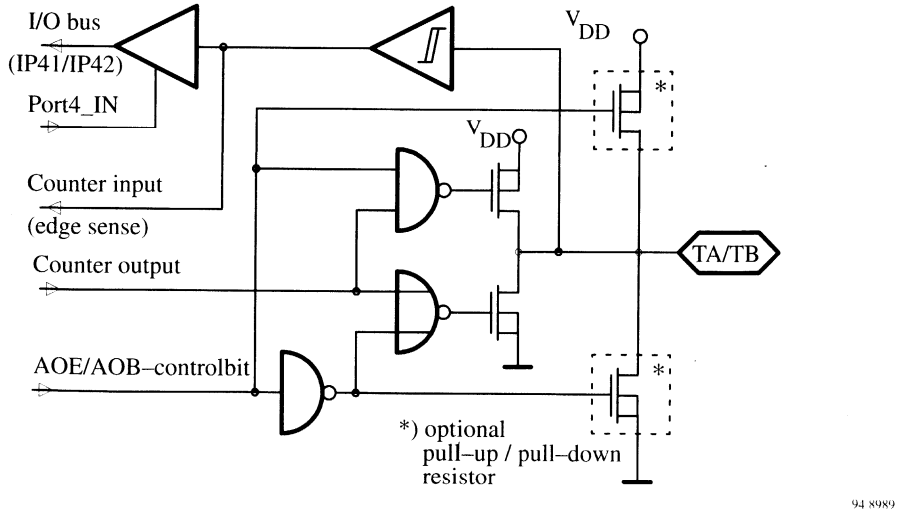


Figure 19. Timer I/O (TA/TB)

2.4 EEPROM

The EEPROM of the M44C260 is 128 bit wide and organized as an array of 16*8-bit. The EEPROM rows are I/O mapped and are subports of port ESUB. The access to any 8-bit row of the EEPROM is done by an extended 8-bit I/O operation or by special postincrement access. The EEPROM rows 12 to 15 can be write protected by hardware and software.

EEPROM SubPort (ESUB)
Address: Bh – Subaddress: 0-Fh

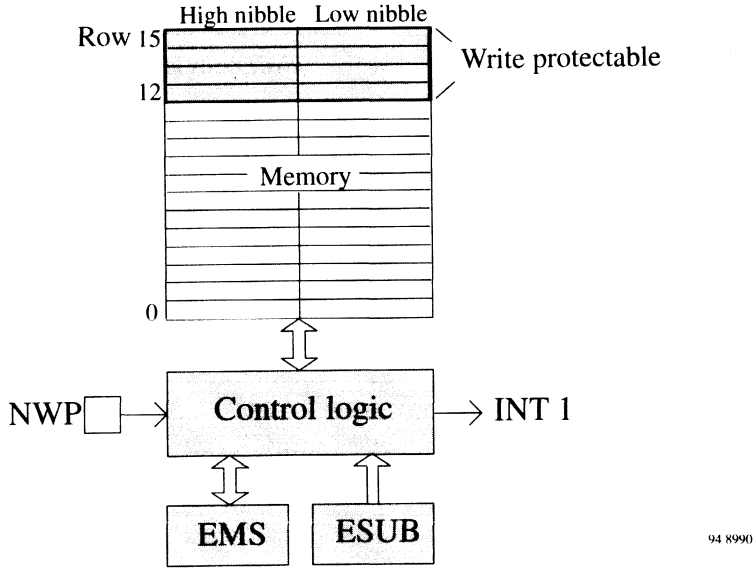


Figure 20. EEPROM

Read operation

A read operation needs an OUT- and two IN-instructions to port ESUB. First the the OUT operation writes the row address. The following two IN-instructions read the high nibble and then the low nibble of the addressed row.

qFORTH example:

Row address	ESUB OUT	(	—)
	EPSUB IN	(	—Data_High)
	EPSUB IN	(Data_High	— Data_High Data_Low)

Write operation

A write operation needs three OUT-instructions to port ESUB. The first operation writes the row address. The following two OUT-instructions write the low nibble and then the high nibble to the addressed row. After reset, rows 12 to 15 are write protected. To enable write operations to these rows the write enable bit (EWE) must be set. In all cases write accesses to these rows are disabled when pin NWP is low.

qFORTH example:

Row address	ESUB OUT	(Data_High Data_Low	— Data_High Data_Low)
	EPSUB OUT	(Data_High Data_Low	—Data_High)
	EPSUB OUT	(Data_High	—)

The internal EEPROM write cycle needs about 16 ms. During this cycle the EEPROM ready bit is reset (EPR = 0). After the data high nibble is written to the port ESUB the internal write cycle is started. During the internal write cycle (while EPR = 0), only read and write accesses to the EMS register are possible. All other EEPROM accesses have no effect.

Postincrement operations

The postincrement mode supports a fast access to consecutive EEPROM rows. A postincrement access is started by setting the EPI bit in the EEPROM mode register (EMS) followed by writing the row start address to port ESUB. After that the read or write operations to the consecutive EEPROM area, beginning at the start address, need only two IN- or OUT-instructions to read or write the data. The row address is incremented automatically after each complete row access (2 nibbles). A write access to the EEPROM mode register (EMS) terminates the postincrement mode.

Note: In the postincrement mode, it is not possible to change from read to write operations or vice versa before the current postincrement operation is finished.

Write ready interrupt (INT1)

At the end of the internal write cycle an interrupt is generated when the interrupt mask bit IMEP in the EEPROM mode register EMS is set. With this interrupt, successive write operations can be executed interrupt controlled within the INT1 interrupt service routine.

2.4.1 EEPROM Mode/Status Register (EMS)

Address: Ah

	Bit 3	2	1	0	
Mode register Write (EMS)	—	**EWE**	**EPI**	**IMEP**	Reset value: 0000b
Status register Read (EMS)	—	—	—	**EPR**	Reset value: xxx1b

EWE EEPROM write enable bit
EWE = 0 disables write accesses to rows 12-15
EWE = 1 enables write accesses to rows 12-15 when the NWP pin is high

EPI EEPROM postincrement mode enable
EPI = 1 activates a postincrement access after the next row address is written to port ESUB

IMEP Interrupt mask for EEPROM write ready interrupt
When IMEP is set an INT1 is generated with the end of the internal EEPROM write cycle

EPR EEPROM ready status flag
EPR = 0 indicates that the EEPROM is not ready for read or write operations (an internal write cycle is executed)
EPR = 1 indicates that the EEPROM is ready for read and write operations

After a write access to the EMS-Register postincrement operations are terminated and any incomplete EEPROM read and write sequence must be started again!

3 Appendix

3.1 Emulation

For emulation all MARC4 controllers have a special emulation mode. It is activated by setting the TE pin to logic HIGH level during reset. In this mode the internal CPU core is inactive and the I/O buses are available via port 0 and port 1 to allow the emulator the access to the on-chip peripherals. The emulator contains a special emulation CPU with a MARC4 core and additional breakpoint logic and takes over the core function. The basic function of the emulator is to evaluate the customer's program and hardware in real time. Thus permits the analysation of any timing, hardware or software problems the simulation of the application. For more informations about emulation see "Emulator Manual".

3.2 MARC4 Instruction Set

The MARC4 instruction set is optimized for the high level programming language qFORTH. A lot of MARC4 instructions are qFORTH words. This enables the compiler to generate fast and compact program code. The MARC4 is a zero address machine with a compact and efficient instruction code. Most of the instructions are single byte instructions. This operations are performed and no source or destination address information. Only BRANCH, CALL and RAM access instructions need address informations and a length of two bytes for long address operations. In all there are five types of instruction formats with a length of one and two bytes.

Zero address operations like arithmetical, logical, shift and rotate operations are performed with data placed on the top of expression stack (TOS and TOS–1). Also I/O– and stack operations are single byte zero address operations and are performed with the top expression stack location.

A literal is a 4-bit constant value which is placed on the data stack. In the MARC4 native code they are represented as LIT_<value>, where <value> is the hexadecimal representation from 0 to 15 (0...F). This range is a result of the MARC4's 4-bit data width. The 6-bit short address and the 12-bit long address formats are both used to address the byte-wide ROM via CALL and conditional branch instructions. This results in a ROM address space of up to 4K*8-bit words.

The MARC4 instruction includes both short and long call instructions as well as conditional branch instructions. On execution the address part of the instructions word are directly loaded into the program counter. Long call and branch instructions can jump anywhere within the program memory area..The lower six bits from the short call (SCALL) and short branch (SBRA) instruction are handled in different way. The six bit SCALL address is multiplied by three and then loaded into the PC. This allows calls within the zero page (000 to 1FFh). The six bit SBRA address is loaded immediately into the lower six bits of the PC. This allows jumps within the 64 byte segment addressed by the upper six bits of the PC.

The CALL and SCALL instructions write the incremented program counter contents to the return stack. This address is loaded back to the PC when the associated EXIT or RTI instruction is encountered. The long RAM address format is used by the four 8-bit RAM address registers which can be pre-increment, post-decrement or loaded directly from the MARC4's internal bus. This results in a direct accessible RAM address space of up to 256 × 4-bit.

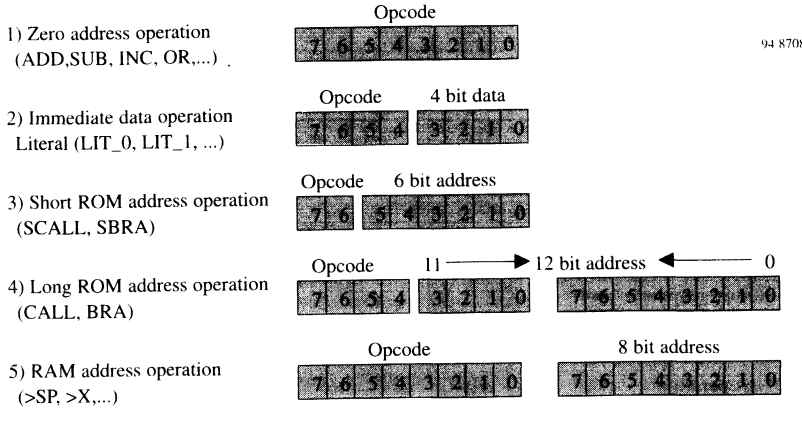


Figure 21. MARC4 Opcode Formats

3.2.1 MARC4 Instruction Set Overview

Mnemonic	Description	Cycles/ Bytes
	Arithmetic operations:	
ADD	Add	1/1
ADDC	Add with carry	1/1
SUB	Subtract	1/1
SUBB	Subtract with borrow	1/1
DAA	Decimal adjust	1/1
INC	Increment TOS	1/1
DEC	Decrement TOS	1/1
DECR	Decrement. 4-bit index on return stack	2/1
	Compare operations:	
CMP_EQ	Compare equal	1/1
CMP_NE	Compare not equal	1/1
CMP_LT	Compare less than	1/1
CMP_LE	Compare less equal	1/1
CMP_GT	Compare greater than	1/1
CMP_GE	Compare greater equal	1/1
	Logical operations:	
XOR	Exclusive OR	1/1
AND	AND	1/1
OR	OR	1/1
NOT	1's complement	1/1
SHL	Shift left into carry	1/1
SHR	Shift right into carry	1/1
ROL	Rotate left through carry	1/1
ROR	Rotate right through carry	1/1
	Flag operations:	
TOG_BF	Toggle branch flag	1/1
SET_BFC	Set branch flag	1/1
DI	Disable all interrupts	1/1
CCR!	Store TOS into CCR	1/1
CCR@	Fetch CCR onto TOS	1/1
	Program branching:	
BRA $xxx	Conditional long branch	2/2
CALL $xxx	Long call (current page)	3/2
SBRA $xxx	Conditional short branch	2/1
SCALL$xxx	Short call (zero page)	2/1
EXIT	Return from subroutine	2/1
RTI	Return from interrupt	2/1
SWI	Software interrupt	1/1
SLEEP	Activate sleep mode	1/1
NOP	No operation	1/1

Mnemonic	Description	Cycles/ Bytes
	Register operations:	
SP@	Fetch the current SP	2/1
RP@	Fetch the current RP	2/1
X@	Fetch the contents of X	2/1
Y@	Fetch the contents of Y	2/1
SP!	Move the top 2 into SP	2/1
RP!	Move the top 2 into RP	2/1
X!	Move the top 2 into X	2/1
Y!	Move the top 2 into Y	2/1
>SP $xx	Store direct address to SP	2/2
>RP $xx	Store direct address to RP	2/2
>X $xx	Store direct address into X	2/2
>Y $xx	Store direct address into Y	2/2
	Stack operations:	
SWAP	Exchange the top 2 nibble	1/1
OVER	Copy TOS-1 to the top	1/1
DUP	Duplicate the top nibble	1/1
ROT	Move TOS-2 to the top	3/1
DROP	Remove the top nibble	1/1
>R	Move the top nibble onto the return stack	1/1
2>R	Move the top 2 nibble onto the return stack	3/1
3>R	Move the top 3 nibble onto the return stack	4/1
R@	Copy 1 nibble from the return stack	1/1
2R@	Copy 2 nibbles from the return stack	2/1
3R@	Copy 3 nibbles from the return stack	4/1
DROPR	Remove the top of return stack (12-Bit)	1/1
LIT_n	Push immediate value (1 nibble) onto TOS	1/1
	ROM data operations:	
TABLE	Fetch 8-bit constant from ROM	3

Mnemonic	Description	Cycles/ Bytes
	Memory operations:	
[X]@ [Y]@	Fetch 1 nibble from RAM indirect addressed by X- or Y-register	1/1
[+X]@ [+Y]@	Fetch 1 nibble from RAM indirect addr. by pre-increm. X- or Y-register	1/1
[X-]@ [Y-]@	Fetch 1 nibble from RAM indirect addr. by post-decrem. X- or Y-register	1/1
[>X]@ $xx [>Y]@ $xx	Fetch 1 nibble from RAM direct addressed by X- or Y-register	2/2
[X]! [Y]!	Store 1 nibble into RAM indirect addressed by [X]	1/1
[+X]! [+Y]!	Store 1 nibble into RAM indirect addressed by pre-incremented [X]	1/1
[X-]! [Y-]!	Store 1 nibble into RAM indirect addr. by post-decrem. X- or Y-register	1/1
[>X]! $xx [>Y]! $xx	Store 1 nibble into RAM direct addressed by X- or Y-register	2/2
	I/O operations:	
IN	Read I/O-Port onto TOS	1/1
OUT	Write TOS to I/O port	1/1

3.2.2 qFORTH Language Overview

MARC4 controller are programmed in the high level language qFORTH which is based upon the FORTH-83 language standard, the **qFORTH** compiler generates native code for a 4-bit FORTH-architecture single chip microcomputer, the TEMIC **MARC4**.**MARC4** applications are all programmed in **qFORTH** which is designed specifically for efficient real time control. Since the qFORTH compiler generates highly optimized code, there is no advantage or point in programming the **MARC4** in assembly code. The high level of code efficiency generated by the qFORTH compiler is achieved by the use of modern optimization techniques such as branch-instruction size minimization, fast procedure calls, pointer tracking and many peephole optimizations.

Langage features:

Expandability
Many of the fundamental qFORTH operations are directly implemented in the MARC4 instruction set.

Stack oriented
All operations communicate with one another via the data stack and use the reverse polish form of notation (RPN)

Structured programming
qFORTH supports structured programming

Reentrant
Different tasks can share the same code.

Recursive
qFORTH routines can call themselves.

Native code inclusion
In qFORTH there is no separation of high level constructs from the native code mnemonics.

3.3 The qFORTH language -Quick Reference Guide

3.3.1 Arithmetic/Logical

-	EXP (n1 n2 — n1-n2)	Subtract the top two values
+	EXP (n1 n2 — n1+n2)	Add up the two top 4-bit values
-C	EXP (n1 n2 — n1+/n+/C)	1's compl. subtract with borrow
+C	EXP (n1 n2 — n1+n2+C)	Add with carry top two values
1+	EXP (n — n+1)	Increment the top value by 1
1-	EXP (n — n–1)	Decrement the top value by 1
2*	EXP (n — n*2)	Multiply the top value by 2
2/	EXP (n — n DIV 2)	Divide the 4-bit top value by 2
D+	EXP (d1 d2 — d1+d2)	Add the top two 8-bit values
D-	EXP (d1 d2 — d1-d2)	Subtract the top two 8-bit values
D2/	EXP (d — d/2)	Divide the top 8-bit value by 2
D2*	EXP (d — d*2)	Multiply the top 8-bit value by 2
M+	EXP (d1 n — d2)	Add a 4-bit to an 8-bit value
M-	EXP (d1 n — d2)	Subtract 4-bit from an 8-bit value
AND	EXP (n1 n2 — n1^n2)	Bitwise AND of top two values
OR	EXP (n1 n2 — n1 v n2)	Bitwise OR the top two values
ROL	EXP (—)	Rotate TOS left through carry
ROR	EXP (—)	Rotate TOS right through carry
SHL	EXP (n — n*2)	Shift TOS value left into carry
SHR	EXP (n — n/2)	Shift TOS value right into carry
NEGATE	EXP (n — –n)	2's complement the TOS value
DNEGATE	EXP (d — –d)	2's complement top 8-bit value
NOT	EXP (n — /n)	1's complement of the top value
XOR	EXP (n1 n2 — n3)	Bitwise Ex-OR the top 2 values

3.3.2 Comparisons

>	EXP (n1 n2 —)	If n1>n2, then branch flag set
<	EXP (n1 n2 —)	If n1<n2, then branch flag set
>=	EXP (n1 n2 —)	If n1>=n2, then branch flag set
<=	EXP (n1 n2 —)	If n1<=n2, then branch flag set
<>	EXP (n1 n2 —)	If n1<>n2, then branch flag set
=	EXP (n1 n2 —)	If n1=n2, then branch flag set
0<>	EXP (n —)	If n <>0, then branch flag set
0=	EXP (n —)	If n = 0, then branch flag set
D>	EXP (d1 d2 —)	If d1>d2, then branch flag set
D<	EXP (d1 d2 —)	If d1<d2, then branch flag set
D>=	EXP (d1 d2 —)	If d1>=d2, then branch flag set
D<=	EXP (d1 d2 —)	If d1<=d2, then branch flag set
D=	EXP (d1 d2 —)	If d1=d2, then branch flag set
D<>	EXP (d1 d2 —)	If d1<>d2, then branch flag set
D0<>	EXP (d —)	If d <>0, then branch flag set
D0=	EXP (d —)	If d =0, then branch flag set
DMAX	EXP (d1 d2 — dMax)	8-bit maximum value of d1, d2
DMIN	EXP (d1 d2 — dMin)	8-bit minimum value of d1, d2
MAX	EXP (n1 n2 — nMax)	4-bit maximum value of n1, n2
MIN	EXP (n1 n2 — nMin)	4-bit minimum value of n1, n2

3.3.3 Control Structures

AGAIN	**EXP (—)**	Ends an infinite loop BEGIN .. AGAIN
BEGIN	**EXP (—)**	BEGIN of most control structures
CASE	**EXP (n — n)**	Begin of CASE .. ENDCASE block
DO	**EXP (limit start —)**	Initializes an iterative DO..LOOP
	RET (— ullimit|start)	
ELSE	**EXP (—)**	Executed when IF condition is false
ENDCASE	**EXP (n —)**	End of CASE..ENDCASE block
ENDOF	**EXP (n — n)**	End of <n> OF .. ENDOF block
EXECUTE	**EXP (ROMAddr —)**	Execute word located at ROMAddr
EXIT	**RET (ROMAddr —)**	Unstructured EXIT from ':'-definition
IF	**EXP (—)**	Conditional IF .. ELSE .. THEN block
LOOP	**EXP (—)**	Repeat LOOP, if index+1<limit
<n> OF	**EXP (c n —)**	Execute CASE block, if n =c
REPEAT	**EXP (—)**	Unconditional branch to BEGIN of BEGIN .. WHILE REPEAT
THEN	**EXP (—)**	Closes an IF statement
UNTIL	**EXP (—)**	Branch to BEGIN, if condition is false
WHILE	**EXP (—)**	Execute WHILE .. REPEAT block, if condition is true
+LOOP	**EXP (n —)**	Repeat LOOP, if I+n < limit
	RET (ullimit|I — ullimit|I+n)	
#DO	**EXP (n —) RET (— ululn)**	Execute the #DO .. #LOOP block n-times
#LOOP	**EXP (—)**	Decrement loop index by 1 downto zero
	RET (ulul|I—ulul|I–1)	
?DO	**EXP (Limit Start —)**	if start=limit, skip LOOP block
?LEAVE	**EXP (—)**	Exit any loop, if condition is true
–?LEAVE	**EXP (—)**	Exit any loop, if condition is false

3.3.4 Stack Operations

0 .. Fh,	**EXP (— n)**	
0 .. 15	**EXP (— n)**	Push 4-bit literal on EXP stack
' <name>	**EXP (— ROMAddr)**	Places ROM address of colon-definition <name> on EXP stack
<ROT	**EXP (n1 n2 n — n n1 n2)**	Move top value to 3rd stack pos.
>R	**EXP (n —) RET (— ululn)**	Move top value onto the return stack
?DUP	**EXP (n — n n)**	Duplicate top value, if n <>0
DEPTH	**EXP (— n)**	Get current expression stack depth
DROP	**EXP (n —)**	Remove the top 4-bit value
DUP	**EXP (n — n n)**	Duplicate the top 4-bit value
I	**EXP (— I) RET (ulul|I — ulul|I)**	Copy loop index I from return to expression stack
J	**EXP (— J)**	Fetch index value of outer loop [2nd return stack level entry]
	RET (ulul|J ulul|I — ulul|J ulul|I)	
NIP	**EXP (n1 n2 — n2)**	Drop second to top 4-bit value
OVER	**EXP (n1 n2 — n1 n2 n1)**	Copy 2nd over top 4-bit value
PICK	**EXP (× — n[x])**	Copy the x-th value from the expression stack onto TOS
RFREE	**EXP (— n)**	Get # of unused RET stack entries
R>	**EXP (— n) RET (ululn —)**	Move top 4-bits from return to expression stack
R@	**EXP (— n)**	Copy top 4-bits from return to expression stack
	RET (ululn — ululn)	
ROLL	**EXP (n —)**	Move n-th value within stack to top

ROT	**EXP (n1 n2 n — n2 n n1)**	Move 3rd stack value to top pos.
SWAP	**EXP (n1 n2 — n2 n1)**	Exchange top two values on stack
TUCK	**EXP (n1 n2 — n2 n1 n2)**	Duplicate top value, move under second item
2>R	**EXP (n1 n2 —)**	Move top two values from expression to return stack
	RET (— u|n2|n1)	
2DROP	**EXP (n1 n2 —)**	Drop top 2 values from the stack
2DUP	**EXP (d — d d)**	Duplicate top 8-bit value
2NIP	**EXP (d1 d2 — d2)**	Drop 2nd 8-bit value from stack
2OVER	**EXP (d1 d2 — d1 d2 d1)**	Copy 2nd 8-bit value over top value
2<ROT	**EXP (d1 d2 d — d d1 d2)**	Move top 8-bit value to 3rd pos'n
2R>	**EXP (— n1 n2)**	Move top 8-bits from return to expression stack
	RET (u|n2|n1 —)	
2R@	**EXP (— n1 n2)**	Copy top 8-bits from return to expression stack
	RET (u|n2|n1 — u|n2|n1)	
2ROT	**EXP (d1 d2 d — d2 d d1)**	Move 3rd 8-bit value to top value
2SWAP	**EXP (d1 d2 — d2 d1)**	Exchange top two 8-bit values
2TUCK	**EXP (d1 d2 — d2 d1 d2)**	Tuck top 8-bits under 2nd byte
3>R	**EXP (n1 n2 n3 —)**	Move top 3 nibbles from the expression onto
	RET (— n3|n2|n1)	the return stack
3DROP	**EXP (n1 n2 n3 —)**	Remove top 3 nibbles from stack
3DUP	**EXP (t — t t)**	Duplicate top 12-bit value
3R>	**EXP (— n1 n2 n3)**	Move top 3 nibbles from return to the expression stack
	RET (n3|n2|n1 —)	
3R@	**EXP (— n1 n2 n3)**	Copy 3 nibbles (1 entry) from the return
	RET (n3|n2|n1 — n3|n2|n1)	to the expression stack

3.3.5 Memory Operations

!	**EXP (n addr —)**	Store a 4-bit value in RAM
@	**EXP (addr — n)**	Fetch a 4-bit value from RAM
+!	**EXP (n addr —)**	Add 4-bit value to RAM contents
1+!	**EXP (addr —)**	Increment a 4-bit value in RAM
1–!	**EXP (addr —)**	Decrement a 4-bit value in RAM
2!	**EXP (d addr —)**	Store an 8-bit value in RAM
2@	**EXP (addr — d)**	Fetch an 8-bit value from RAM
D+!	**EXP (d addr —)**	Add 8-bit value to byte in RAM
D–!	**EXP (d addr —)**	Subtract 8-bit value from a byte in RAM
DTABLE@	**EXP (ROMAddr n — d)**	Indexed fetch of a ROM constant
DTOGGLE	**EXP (d addr —)**	Exclusive-OR 8-bit value with byte in RAM
ERASE	**EXP (addr n —)**	Sets n memory cells to 0
FILL	**EXP (addr n n1 —)**	Fill n memory cells with n1
MOVE	**EXP (n from to —)**	Move a n-digit array in memory
ROMByte@	**EXP (ROMAddr — d)**	Fetch an 8-bit ROM constant
TOGGLE	**EXP (n addr —)**	Ex-OR value at address with n
3!	**EXP (nh nm nl addr —)**	Store 12-bit value into a RAM array
3@	**EXP (addr — nh nm nl)**	Fetch 12-bit value from RAM
T+!	**EXP (nh nm nl addr —)**	Add 12-bits to 3 RAM cells
T–!	**EXP (nh nm nl addr —)**	Subtract 12-bits from 3 nibble RAM array
TD+!	**EXP (d addr —)**	Add byte to a 3 nibble RAM array
TD–!	**EXP (d addr —)**	Subtract byte from 3 nibble array

3.3.6 Predefined Structures

(ccccccc)		In-line comment definition
\ ccccccc		Comment until end of the line
: <name>	**RET (—)**	Begin of a colon definition
;	**RET (ROMAddr —)**	Exit; ends any colon definition
[FIRST]	**EXP (— 0)**	Index (=0) for first array element
[LAST]	**EXP (— nId)**	Index for last array element
CODE	**EXP (—)**	Begins an in-line macro definition
END-CODE	**EXP (—)**	Ends an In-line macro definition
ARRAY	**EXP (n —)**	Allocates space for a 4-bit array
2ARRAY	**EXP (n —)**	Allocates space for an 8-bit array
CONSTANT	**EXP (n —)**	Defines a 4-bit constant
2CONSTANT	**EXP (d —)**	Defines an 8-bit constant
LARRAY	**EXP (d —)**	Allocates space for a long 4-bit array with up to 255 elements
2LARRAY	**EXP (d —)**	Allocates space for a long byte array
Index	**EXP (nId addr—addr')**	Run-time array access using a variable array index
ROMCONST	**EXP (—)**	Define ROM look-up table with 8-bit values
VARIABLE	**EXP (—)**	Allocates memory for 4-bit value
2VARIABLE	**EXP (—)**	Creates an 8-bit variable
<n> ALLOT		Allocate space for <n+1> nibbles of un-initialized RAM
AT <address>		Fixed <address> placement
: INTx	**RET (— ROMAddr)**	Interrupt service routine entry
$AutoSleep		Entry point address on return stack underflow
: $RESET	**EXP (—)**	Entry point on power-on reset

3.3.7 Assembler Mnemonics

ADD	**EXP (n1 n2 — n1+n2)**	Add the top two 4-bit values
ADDC	**EXP (n1 n2 — n1+n2+C)**	Add with carry top two values
CCR!	**EXP (n —)**	Write top value into the CCR
CCR@	**EXP (— n)**	Fetch the CCR onto top of stack
CMP_EQ	**EXP (n1 n2 — n1)**	If n1=n2, then branch flag set
CMP_GE	**EXP (n1 n2 — n1)**	If n1>=n2, then branch flag set
CMP_GT	**EXP (n1 n2 — n1)**	If n1>n2, then branch flag set
CMP_LE	**EXP (n1 n2 — n1)**	If n1<=n2, then branch flag set
CMP_LT	**EXP (n1 n2 — n1)**	If n1<n2, then branch flag set
CMP_NE	**EXP (n1 n2 — n1)**	If n1<>n2, then branch flag set
CLR_BCF	**EXP (—)**	Clear branch and carry flag
SET_BCF	**EXP (—)**	Set branch and carry flag
TOG_BF	**EXP (—)**	Toggle the branch flag
DAA	**EXP (n>9 or C set — n+6)**	BCD arithmetic adjust [addition]
DAS	**EXP (n — 10+/n+C)**	9's complement for BCD subtract
DEC	**EXP (n — n–1)**	Decrement top value by 1
DECR	**RET (ulull — ulull–1)**	Decrement value on the return stack
DI	**EXP (—)**	Disable interrupts
DROPR	**RET (ululu —)**	Drop element from return stack
EXIT	**RET (ROMAddr —)**	Exit from current ':'-definition
EI	**EXP (—)**	Enable interrupts
IN	**EXP (port — data)**	Read data from an I/O port
INC	**EXP (n — n+1)**	Increment the top value by 1
NOP	**EXP (—)**	No operation
NOT	**EXP (n — /n)**	1's complement of the top value

RP!	**EXP (d —)**	Store as return stack pointer
RP@	**EXP (— d)**	Fetch current RET stack pointer
RTI	**RET (RETAddr —)**	Return from interrupt routine
SLEEP	**EXP (—)**	Enter 'sleep-mode', enable all interrupts
SWI0 SWI7	**EXP (—)**	Software triggered interrupt
SP!	**EXP (d —)**	Store as stack pointer
SP@	**EXP (— d)**	Fetch current stack pointer
SUB	**EXP (n1 n2 — n1-n2)**	2's complement subtraction
SUBB	**EXP (n1 n2 — n1+/n2+C)**	1's compl. subtract with borrow
TABLE	**EXP (— d)**	
	RET (RetAddr RomAddr —)	Fetches an 8-bit constant from an address in ROM
OUT	**EXP (data port —)**	Write data to I/O port
X@	**EXP (— d)**	Fetch current × register contents
[X]@	**EXP (— n)**	Indirect × fetch of RAM contents
[+X]@	**EXP (— n)**	Pre-incr. × indirect RAM fetch
[X–]@	**EXP (— n)**	Postdecr. × indirect RAM fetch
[>X]@ $xx	**EXP (— n)**	Direct RAM fetch, × addressed
X!	**EXP (d —)**	Move 8-bit address to × register
[X]!	**EXP (n —)**	Indirect × store of RAM contents
[+X]!	**EXP (n —)**	Pre-incr. × indirect RAM store
[X–]!	**EXP (n —)**	Postdecr. × indirect RAM store
[>X]! $xx	**EXP (n —)**	Direct RAM store, × addressed
Y@	**EXP (— d)**	Fetch current Y register contents
[Y]@	**EXP (— n)**	Indirect Y fetch of RAM contents
[+Y]@	**EXP (— n)**	Pre-incr. Y indirect RAM fetch
[Y–]@	**EXP (— n)**	Postdecr. Y indirect RAM fetch
[>Y]@ $xx	**EXP (— n)**	Direct RAM fetch, Y addressed
Y!	**EXP (d —)**	Move address to Y register
[Y]!	**EXP (n —)**	Indirect Y store of RAM contents
[+Y]!	**EXP (n —)**	Pre-incr. Y indirect RAM store
[Y–]!	**EXP (n —)**	Postdecr. Y indirect RAM store
[>Y]! $xx	**EXP (n —)**	Direct RAM store, Y addressed
>RP $xx	**EXP (—)**	Set return stack pointer
>SP $xx	**EXP (—)**	Set expression stack pointer
>X $xx	**EXP (—)**	Set × register immediate
>Y $xx	**EXP (—)**	Set Y register immediate

Notes:

RET (–)	Return address stack effects
EXP (–)	Expression (or data) stack effects
True condition	Means branch flag set in CCR
False condition	Means branch flag reset in CCR
n	4-bit data value
d	8-bit data value
addr	8-bit RAM address
ROMaddr	12-bit ROM address

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Voltages are given relative to V_{SS}.

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	– 0.3 to + 7.0	V
Input voltage (on any pin)	V_{IN}	V_{SS} –0.3 ≤ V_{IN} ≤ V_{DD} +0.3	V
Output short circuit duration	t_{short}	indefinite	sec
Operating temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	T_{stg}	–40 to +130	°C
Thermal resistance (PLCC)	R_{thJA}	110	K/W
Soldering temperature (t ≤ 10 s)	T_{sd}	260	°C

Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operational the device at any condition above those indicated in the operational section of these specification is not implied. Exposure to absolute maximum rating condition for an extended period may affect device reliability. All inputs and outputs are protected against high electrostatic voltages or electric fields. However, precautions to minimize built-up of electrostatic charges during handling are recommended. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., V_{DD}).

4.2 DC Operating Characteristics

Supply voltage V_{DD} = 2.4 to 6.2 V, V_{SS} = 0 V, T_{amb} = –40 to 85°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Active current (CPU active)	V_{DD} = 2.4 V f_{SYSCL}=1MHz	I_{DD}			1.0	mA
	f_{SYSCL}=2MHz				2.0	mA
	V_{DD} = 6.2 V f_{SYSCL}=1MHz				2.6	mA
	f_{SYSCL}=2MHz				5.2	mA
Power down current (CPU sleep, RC oscillator active)	V_{DD} = 2.4 V f_{SYSCL}=1MHz	I_{PD}			0.4	mA
	f_{SYSCL}=2MHz				0.8	mA
	V_{DD} = 6.2 V f_{SYSCL}=1MHz				0.6	mA
	f_{SYSCL}=2MHz				1.0	mA
Sleep current (CPU sleep, RC oscillator inactive)	V_{DD} = 2.4 V	I_{Sleep}			1.0	µA
	V_{DD} = 6.2 V				1.0	µA
Sleep current (CPU sleep, RC oscillator inactive)	V_{DD} = 2.4 V V_{DD} = 6.2 V T_{amb} = 25°C	I_{Sleep}			0.5	µA
					0.5	µA

Supply voltage V_{DD} = 2.4 to 6.2 V, V_{SS} = 0 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power-on reset threshold voltage: Note x figure xx						
POR threshold voltage		V_{POR}	1.5		2.1	V
POR hysteresis		ΔV_{POR}		100		mV
Schmitt-trigger input voltage: Pin INT6, TA, TB, port 40 and port 3						
Negative-going threshold voltage	V_{DD} = 2.4 to 6.2 V	V_{T-}	V_{SS}		0.3*V_{DD}	V
Positive-going threshold voltage	V_{DD} = 2.4 to 6.2 V	V_{T+}	0.7*V_{DD}		V_{DD}	V
Hysteresis (VT ± VT–)	V_{DD} = 2.4 to 6.2 V	V_H		0.1*V_{DD}		
Input voltage: Pin NRST, TE, NWP, TCL, and port 0, 1, 2, port 43:						
Input voltage LOW	V_{DD} = 2.4 to 6.2 V	V_{IL}	V_{SS}		0.2*V_{DD}	V
Input voltage HIGH	V_{DD} = 2.4 to 6.2 V	V_{IH}	0.8*V_{DD}		V_{DD}	V
Input current: Bidirectional ports 0, 1, 2, 3, input port 4 with pull-up resistor Pin NRST, TCL, INT6						
Input LOW current	V_{DD}= 2.4 V V_{IL}= V_{SS} V_{DD}= 6.2 V	I_{IL}	–2.7 –28	–6.7 –60	–13 –103	µA µA
Input current: Bidirectional ports 0, 1, 2, 3, input port 4 with pull-down resistor Pin TE, NWP, TA, TB						
Input HIGH current	V_{DD} = 2.4 V V_{IH} = V_{DD} V_{DD} = 6.2 V	I_{IH}	2.7 30	6.3 60	12 100	µA µA
Output current: Bidirectional ports 0, 1, 2, 3 and TA, TB						
Output LOW current	V_{DD} = 2.4 V V_{OL} = 0.2*V_{DD} V_{DD} = 6.2 V	I_{OL}	0.8 6	1.6 11	2.8 17	mA mA
Output HIGH current	V_{DD} = 2.4 V V_{OH} = 0.8*V_{DD} V_{DD} = 6.2 V	I_{OH}	–0.6 –4	–1.3 –7.5	–2.2 –12	mA mA
Output current: Pin TCL						
Output LOW current	V_{DD} = 2.4 V V_{OL} = 0.2*V_{DD} V_{DD} = 6.2 V	I_{OL}	1.6 12	3.2 22	5.6 34	mA mA
Output HIGH current	V_{DD} = 2.4 V V_{OH} = 0.8*V_{DD} V_{DD} = 6.2 V	I_{OH}	–1.2 –8	–2.6 –15	–4.4 –24	mA mA

4.3 AC Characteristics

Supply voltage V_{DD} = 2.4 to 6.2 V, V_{SS} = 0 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Timer 2A and 2B input timing						
Timer input clock		f_{TI}			SYSCL	–
Timer input LOW time	Rise/fall time < 10 ns	t_{TIL}	50			ns
Timer input HIFG time	Rise/fall time < 10 ns	t_{TIH}	50			ns
Interrupt request input timing						
Int. request LOW time	Rise/fall time < 10 ns	t_{IRL}	50			ns
Int. request HIGH time	Rise/fall time < 10 ns	t_{IRH}	50			ns
TCL clock						
TCL input clock		f_{TCL}			2	MHz
TCL input LOW time		t_{TCLL}	250			ns
TCL input HIGH time		t_{TCLH}	0.250		10	µs
TCL rise time		t_{TCLR}			10	ns
TCL fall time		t_{TCLF}				
Reset timing						
Power-on reset time		T_{POR}		100	500	µs
NRES input LOW time		T_{POR}	4*SYSCL			µs
EEPROM write cycle						
EEPROM write time	Note 1	t_{EEW}		16		ms
EEPROM write cycles		n_W	$5*10^5$	10^6		–
Operation cycle time						
System clock cycle	CCS = 1 Note 1 CCS = 0	t_{SYSCL}		477 954		ns ns
RC oscillator						
Frequency	Note 1	f_{RCI}		1048		kHz
Stability	Note 1	Δf/f		2000		ppm
Stabilization time	Note 1	t_S		1000		s
32 kHz oscillator						
Frequency		f_X		32.768		kHz
Start up time		t_{SQ}				s
Stability	Note 2	Δf/f	–10		10	ppm
Integrated input/output capacitances		C_{IN} C_{OUT}		10		pF
External 32 kHz crystal parameters						
Crystal frequency		f_X		32.768		kHz
Series resistance		RS		30	50	kΩ
Static capacitance		C0		1.5		pF
Dynamic capacitance		C1		3		fF

Note 1: With connected crystal (pin 5, 6) and after start up time of crystal oscillator.

Note 2: Depend on the connected quartz crystal.

Crystal

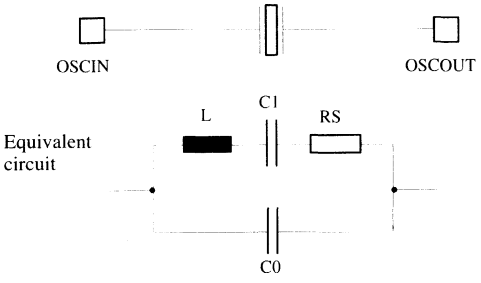


Figure 22. Equivalent crystal circuit

Power-on reset

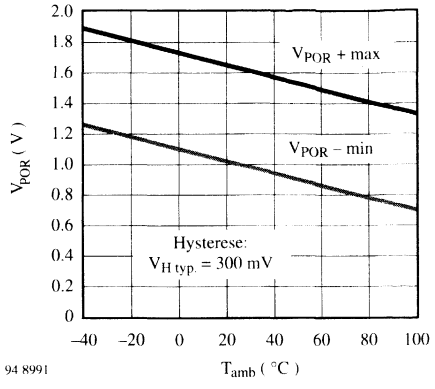


Figure 23. Thresholds for POR vs. ambient temperature

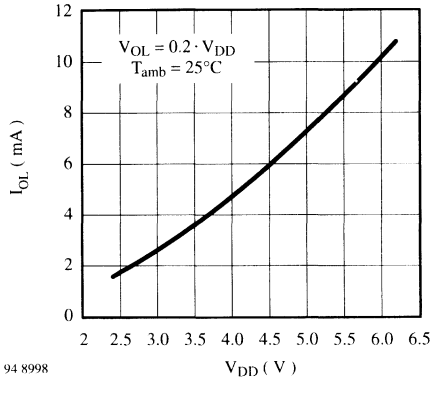


Figure 24. Output LOW current vs. supply voltage

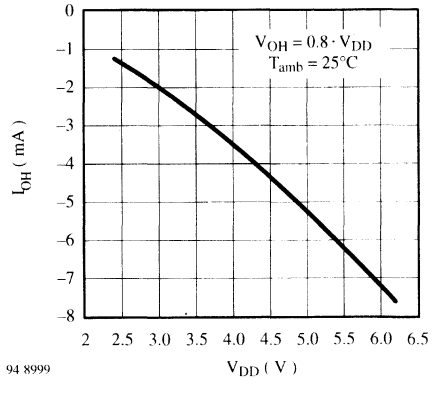


Figure 26. Output HIGH current vs. supply voltage

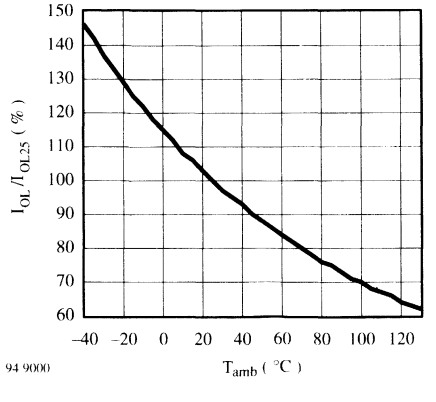


Figure 25. Output LOW current standardized to 25°C vs. temp.

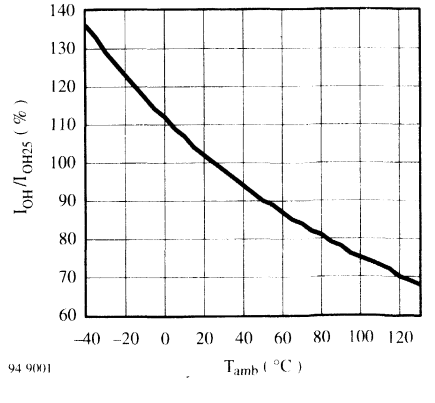


Figure 27. Output HIGH current standardized to 25°C vs temp.

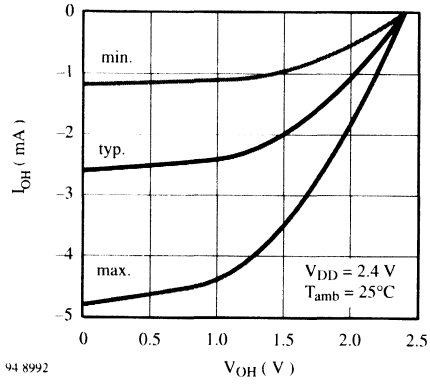


Figure 28. Output HIGH current vs. output HIGH voltage

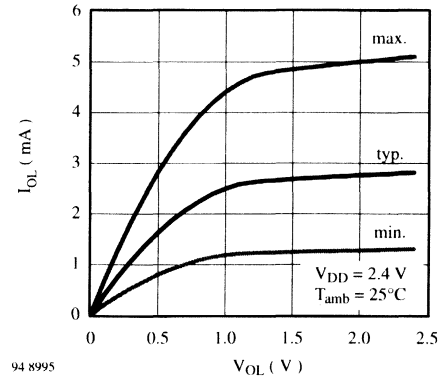


Figure 31. Output LOW current vs. output LOW voltage

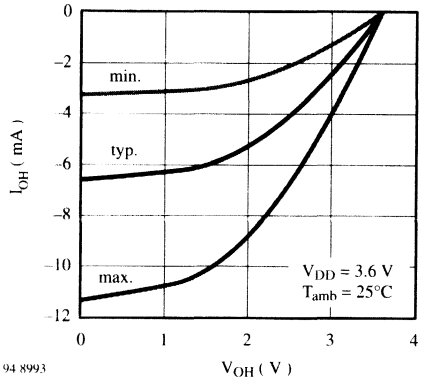


Figure 29. Output HIGH current vs. output HIGH voltage

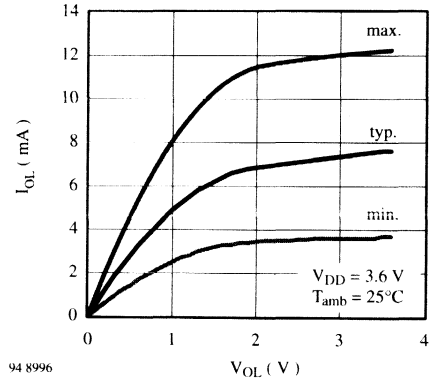


Figure 32. Output LOW current vs. output LOW voltage

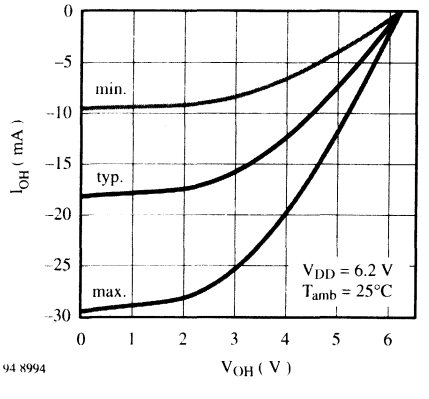


Figure 30. Output HIGH current vs. output HIGH voltage

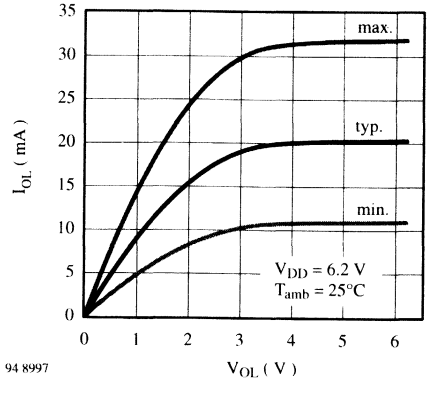


Figure 33. Output LOW current vs. output LOW voltage

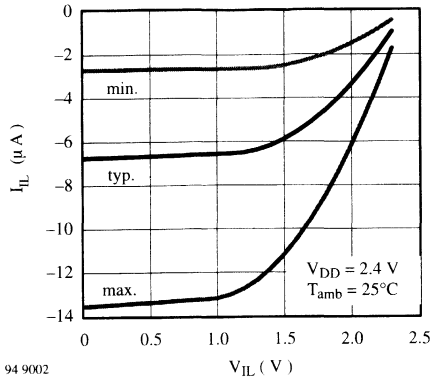


Figure 34. Input LOW current vs. input LOW voltage

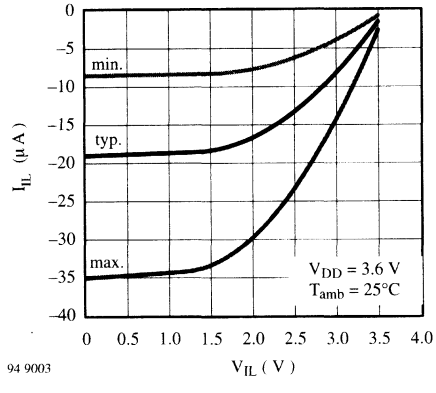


Figure 35. Input LOW current vs. input LOW voltage

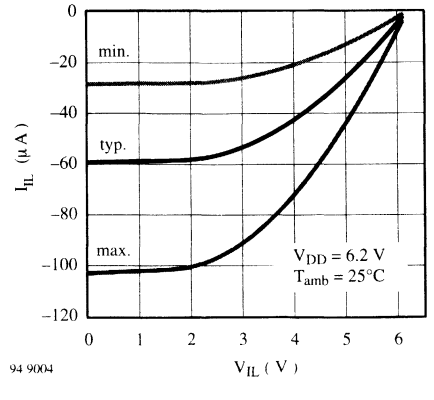


Figure 36. Input LOW current vs. input LOW voltage

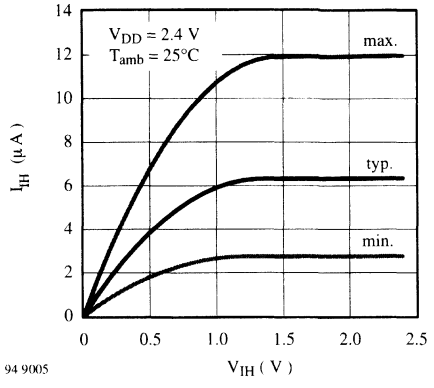


Figure 37. Input HIGH current vs. input HIGH voltage

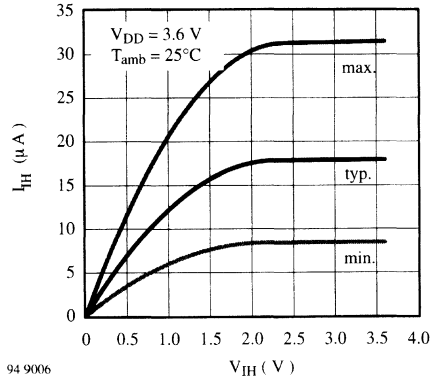


Figure 38. Input HIGH current vs. input HIGH voltage

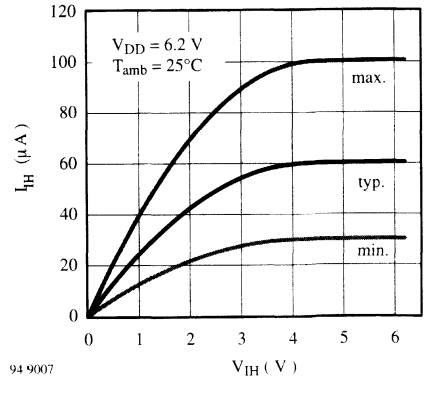


Figure 39. Input HIGH current vs. input HIGH voltage

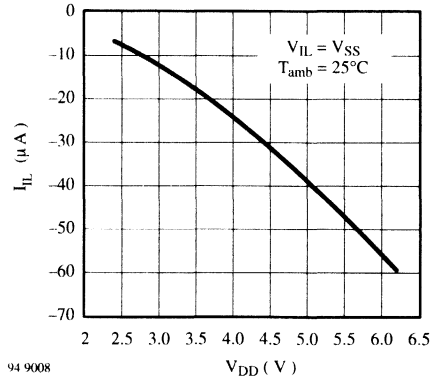


Figure 40. Input LOW current vs. supply voltage

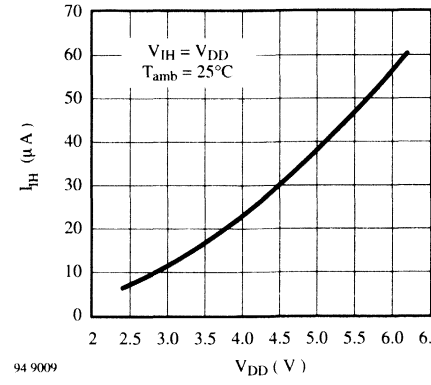


Figure 42. Input HIGH current vs. supply voltage

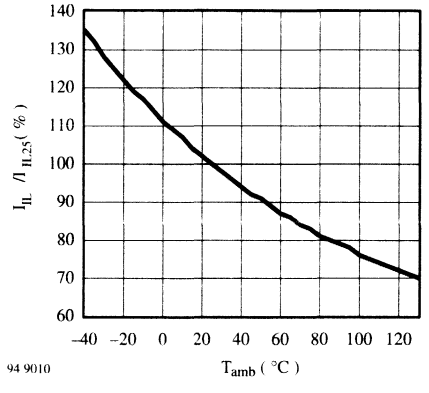


Figure 41. Input LOW current standardized to 25°C vs. temperature

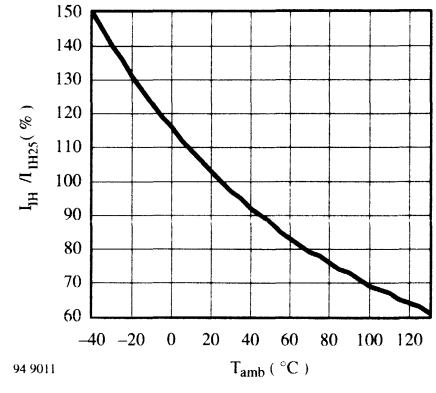


Figure 43. Input HIGH current standardized to 25°C vs. temperature

4.4 Schmitt-Trigger Inputs

The following figures show the Schmitt-trigger input specs used at timer inputs TA, TB and interrupt inputs.

Note: The values for switch levels are standardized to supply voltage.

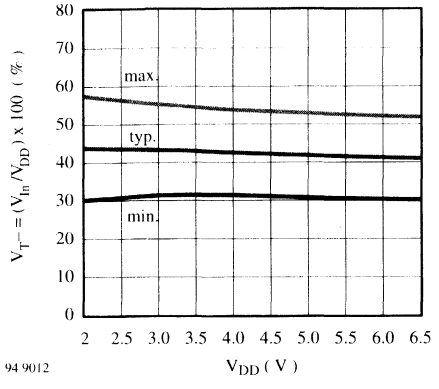


Figure 44. Schmitt-trigger positive going threshold voltage

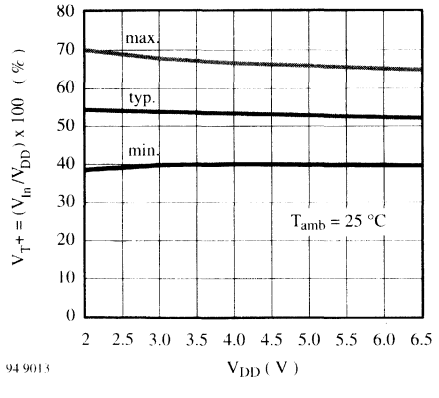


Figure 45. Schmitt-trigger negative going threshold voltage

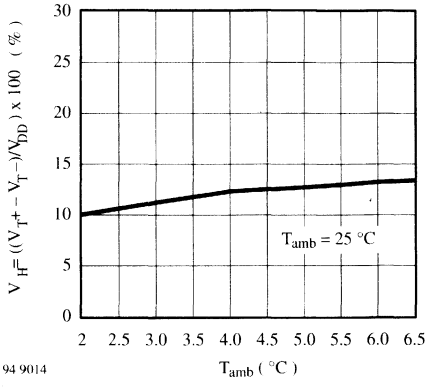


Figure 46. Schmitt-trigger hysteresis vs. supply voltage

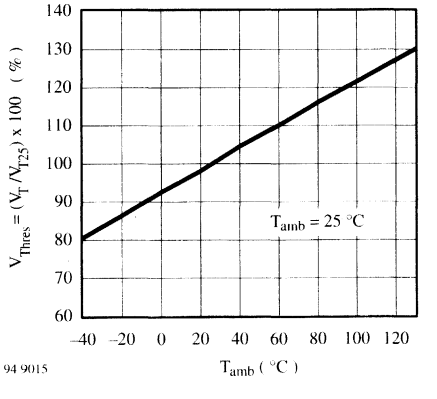


Figure 47. Threshold temperature drift

Note: For a pulse to be recognizable, it must be a minimum of 50 ns long with a rise time ≤ 10 ns.

5 Pad Layout

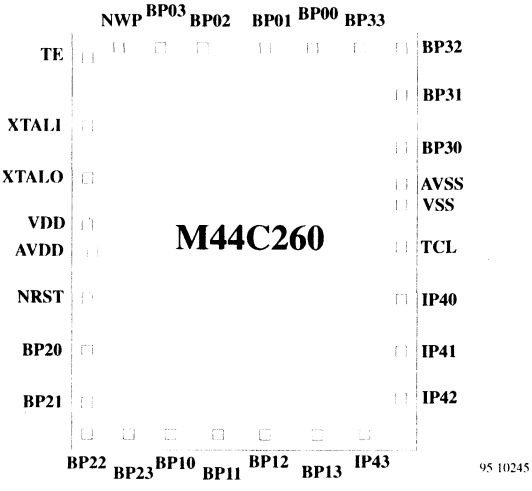


Figure 48. Pad Layout

Table 8. Pad coordinates

Number	Name	X point	Y point	Number	Name	X point	Y point
1	BP22	0,0	0,0	16	BP32	3056,0	3741,5
2	BP23	404,5	0,0	17	BP33	2651,5	3741,5
3	BP10	809,0	0,0	18	BP00	2247,0	3741,5
4	BP11	1398,5	0,0	19	BP01	1830,5	3741,5
5	BP12	1811,0	0,0	20	BP02	1136,5	3741,5
6	BP13	2223,5	0,0	21	BP03	720,0	3741,5
7	IP43	2686,5	0,0	22	NWP	303,5	3741,5
8	IP42	3056,0	509,0	23	TE	0,0	3660,0
9	IP41	3056,0	965,0	24	XTALI	0,0	3103,0
10	IP40	3056,0	1363,0	25	XTALO	0,0	2625,0
11	TCL	3056,0	1802,0	26	VDD dig.	0,0	2315,0
12	VSS	3056,0	2247,5	27	VDD ana.	24,0	2044,0
13	AVSS	3056,0	2457,5	28	NRST	0,0	1707,0
14	BP30	3056,0	3301,0	29	BP20	0,0	1164,5
15	BP31	3056,0	3741,5	30	BP21	0,0	424,5

The M44C260 is also available in the form for COB mounting. Therefore the substrate, i.e., the backside of the die, sould be connected to V_{SS}.

Die size: 3.51mm x 4.19 mm

Pad size: 90 µm * 90 µm

Thickness: 480 ± 25 µm

6 Ordering Information

Pin options

Please select the option setting from the list below.

Pin	Output		Input	
	CMOS	Open Drain	Pull Up	Pull Down
BP00				
BP01				
BP02				
BP03				
BP10				
BP11				
BP12				
BP13				
BP20				
BP21				
BP22				
BP23				
BP30				
BP31				
BP32				
BP33				
IP40–INT6				
IP41–TA				
IP42–TB				
IP43				
NWP				
TE				

ROM code

Please insert ROM CRC.

Size: _____ KByte **CRC:** _____ hex

Approval

Date: _____ Signature: _____

MARC4 – 4-bit Microcontroller

The M48C260 is a member of the TEMIC family of 4-bit single chip microcontrollers. It is the user programmable version of the M44C260. It contains EEPROM progra,m memory, RAM, EEPROM data memory, parallel I/O ports, 1 timer with watchdog function, 2 × 8/16-bit multifunction timer/counter and the on-chip clock generation.

Features

- 4-bit HARVARD architecture
- 1 µs instruction cycle
- 4K × 8-bit application EEPROM program memory
- 256 × 4-bit RAM
- 16 × 8-bit EEPROM
- 16 bidirectional I/O's
- 8 hard and software interrupt levels
- 2 × 8-bit multifunction timer/counter
- Interval timer with watchdog
- 32 kHz on-chip oscillator

Benefits

- Low power consumption
- Power down mode < 1 µA
- 2.4 to 6.2 V supply voltage
- Self test functions
- High level programming language in qFORTH
- User programmable with the application program

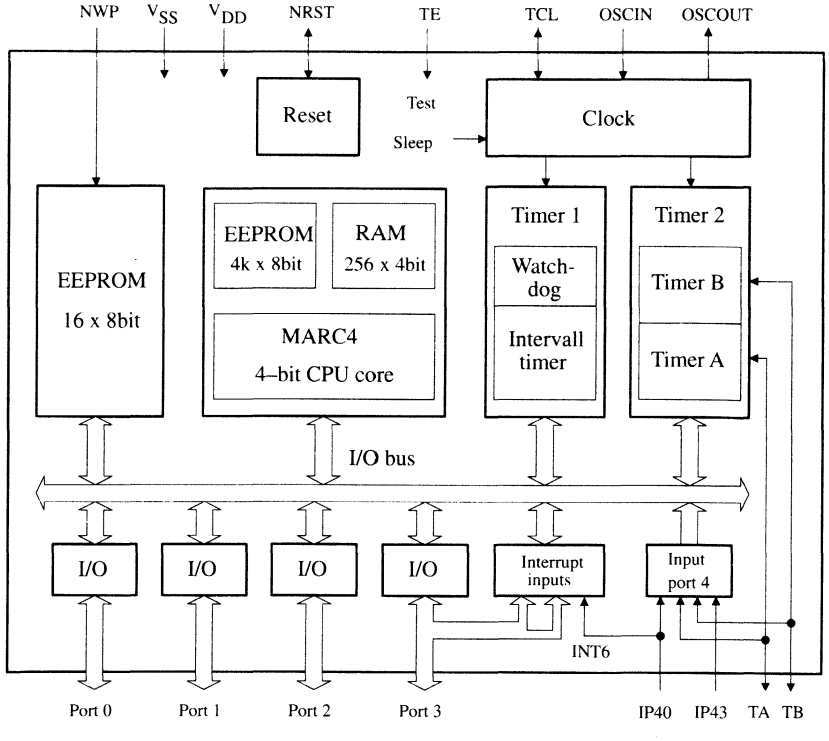


Figure 1. Block diagram

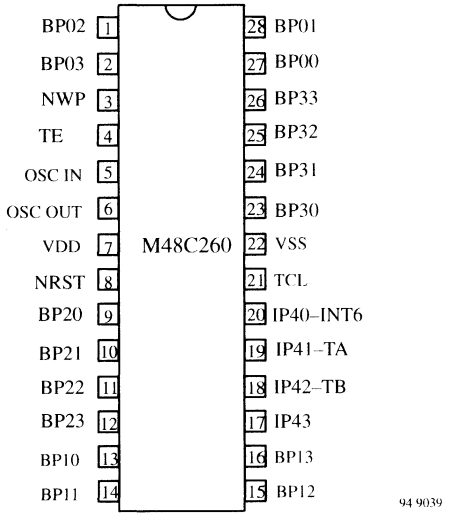


Figure 2. Pin connections

Table 1. Pin description

Name	Function
V_{DD}	Power supply voltage +2.4 to +6.2 V
V_{SS}	Circuit ground
BP00 – BP03	4 bidirectional I/O lines of port 0 *
BP10 – BP13	4 bidirectional I/O lines of port 1 *
BP20 – BP23	4 bidirectional I/O lines of port 2 *
BP30 – BP33	4 bidirectional I/O lines of port 3 with alternate interrupt function. A negative transition on BP30/BP31 requests an INT2-, and on BP32/BP33 an INT3-interrupt if the corresponding interrupt-mask is set.
IP40-INT6	Input port 40 line/interrupt 6 input * A negative transition on this input requests an INT6 interrupt if the IM6 mask bit is set.
IP41-TA	Timer/counter I/O/Input port 41 line * This line can be used as programmable I/O of counter A or as port 41 input.
IP42-TB	Timer/counter I/O/input port 42 line * This line can be used as programmable I/O of counter B or as port 42 input.
IP43	Input port 43 line *)
NWP	EEPROM write protect input, a logic low on this input protects EEPROM rows 12 to 15.
OSCIN	Oscillator input (32-kHz crystal).
OSCOUT	Oscillator output (32-kHz crystal).
NRST	Reset input/output, a logic low on this pin resets the device. An internal watchdog reset is indicated by a low level on this pin.
TCL	External system clock I/O. This pin can be used as input to provide the C with an external clock or as output of the internal system clock.
TE	Testmode input. This input is used to control the test modes and the function of the TCL pin.

*) The I/O ports have CMOS output buffers. As input they are available with pull-up or pull-down resistors. Please see the order information.

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Table of Contents (continued)

1 MARC4 Architecture

1.1 General Description

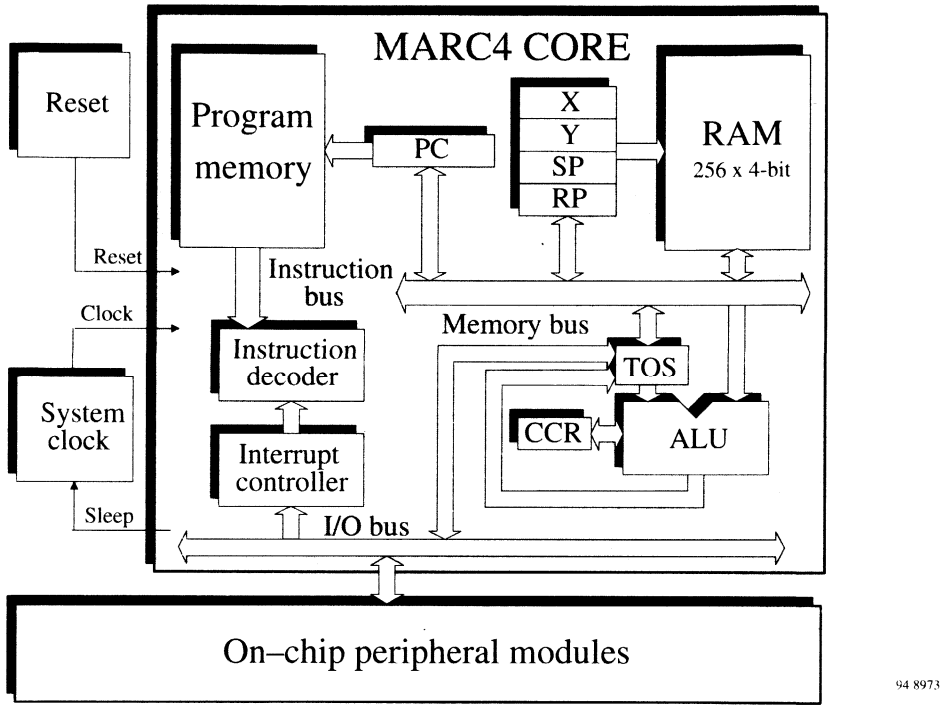


Figure 3. MARC4 core

The MARC4 microcontroller consists of an advanced stack based 4-bit CPU core and on-chip peripherals. The CPU is based on the HARVARD architecture with physically separate program memory (EEPROM) and data memory (RAM). Three independent buses, the instruction bus, the memory bus and the I/O bus are used for parallel communication between ROM, RAM and peripherals. This enhances program execution speed by allowing both instruction prefetching, and a simultaneous communication to the on-chip peripheral circuitry. The integrated powerful interrupt controller with eight prioritized interrupt levels, supports fast processing of hardware events.

The MARC4 is designed for the high level programming language qFORTH. The core contains both FORTH stacks, expression stack and return stack. This architecture allows high level language programming without any loss in efficiency or code density.

1.2 Components of MARC4 Core

The core contains program memory, RAM, ALU, program counter, RAM address register, instruction decoder and interrupt controller. The following sections describe each of this parts.

1.2.1 Program Memory (EEPROM)

The program memory (EEPROM) is programmed with the application program by the customer using a special programming device (see capter "Progamming the EEPROM Program Memory"). The ROM is addressed by a 12-bit wide program counter, thus limiting the program size to a maximum of 4 Kbytes. An additional 1 Kbyte ROM is available for test software only.

The EEPROM starts with a 512 byte segment (zero page) which contains predefined start addresses for interrupt service routines and special subroutines accessible with single byte instructions (SCALL). The corresponding memory map is shown in figure 4.

Look-up tables of constants can also be held in EEPROM and are accessed via the MARC4's built-in TABLE instruction.

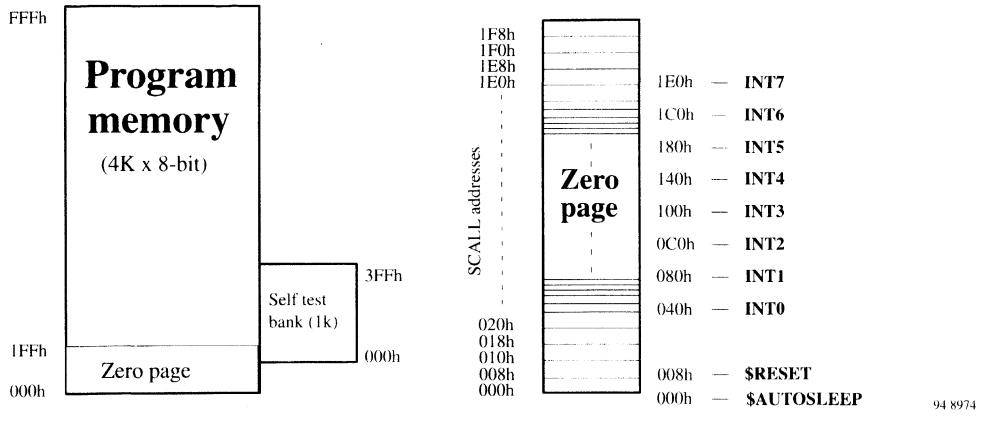


Figure 4. Progam memory map

1.2.2 Data Memory (RAM)

The MARC4 contains 256 x 4-bit wide static random access memory (RAM). It is used for the expression stack, the return stack and data memory for variables and arrays. The RAM is addressed by any of the four 8-bit wide RAM address registers SP, RP, X and Y.

- Expression Stack

The 4-bit wide expression stack is addressed with the expression stack pointer (SP). All arithmetic, I/O and memory reference operations take their operands from, and return their result to the expression stack. The MARC4 performs the operations with the top of stack items (TOS and TOS-1). The TOS register contains the top element of the expression stack and works like an accumulator. This stack is also used for passing parameters between subroutines, and as a scratchpad area for temporary storage of data.

- Return Stack

The 12-bit wide return stack is addressed by the return stack pointer (RP). It is used for storing return addresses of subroutines, interrupt routines and for keeping loop index counts. The return stack can also be used as a temporary storage area.

The MARC4 instruction set supports the exchange of data between the top elements of the expression stack and the return stack. The two stacks within the RAM have a user definable location and maximum depth.

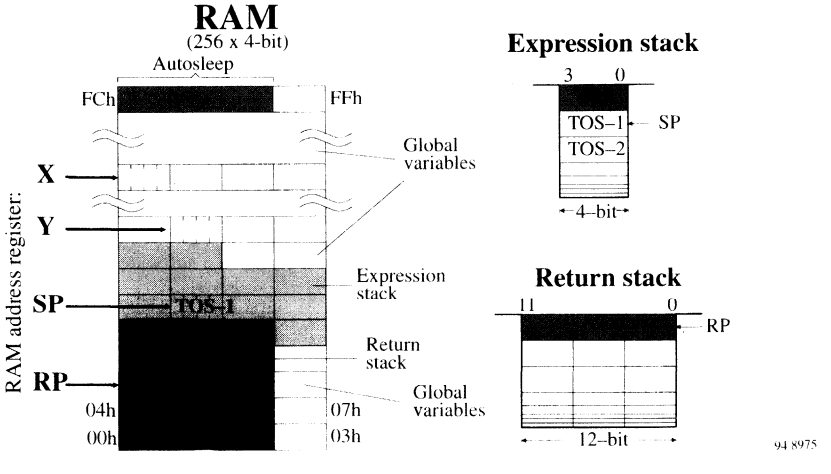


Figure 5. RAM map

1.2.3 Registers

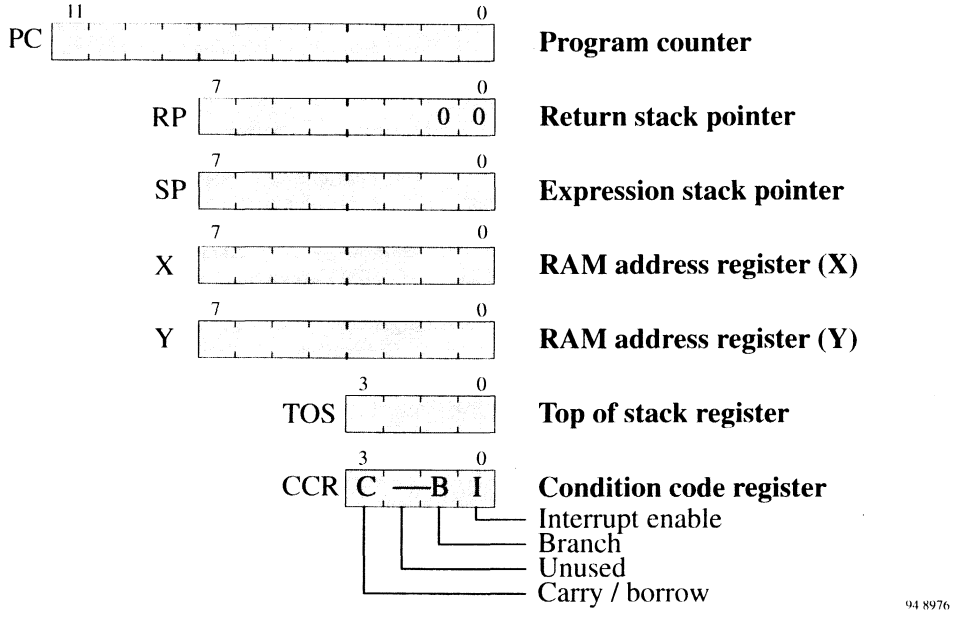


Figure 6. Programming model

The MARC4 controller has six programmable registers and one condition code register. They are shown in the following programming model.

- Program Counter (PC)

The program counter (PC) is a 12-bit register that contains the address of the next instruction to be fetched from the program memory. Instructions currently being executed are decoded in the instruction decoder to determine the internal micro operations. For linear code (no calls or branches) the program counter is incremented with every instruction cycle. If a branch-, call-, return-instruction or an interrupt is executed the program counter is loaded with a new address. The program counter is also used with the TABLE instruction to fetch 8-bit wide ROM constants.

RAM address register

The RAM is addressed with the four 8-bit wide RAM address registers: SP, RP, X and Y. These registers allow access to any of the 256 RAM nibbles.

- Expression Stack Pointer (SP)

The stack pointer (SP) contains the address of the next-to-top 4-bit item (TOS-1) of the expression stack. The pointer is automatically pre-incremented if a nibble is moved onto the stack or post-decremented if a nibble is removed from the stack. Every post-decrement operation moves the item (TOS-1) to the TOS register before the SP is decremented. After a reset the stack pointer has to be initialized with " >SP $xx " to allocate the start address of the expression stack area.

- Return Stack Pointer (RP)

The return stack pointer points to the top element of the 12-bit wide return stack. The pointer automatically pre-increments if an element is moved onto the stack or it post-decrements if an element is removed from the stack. The return stack pointer increments and decrements in steps of 4. This means that every time a 12-bit element is stacked, a 4-bit RAM location are left unwritten. These location are used by the qFORTH compiler to allocate 4-bit variables. After a reset the return stack pointer has to be initialized with " >RP FCh ".

- RAM Address Register (X and Y)

The X and Y registers are used to address any 4-bit item in the RAM. A fetch operation moves the addressed nibble onto the TOS. A store operation moves the TOS to the addressed RAM location. Using either the pre-increment or post-decrement addressing mode arrays in the RAM can be compared, filled or moved.

- Top Of Stack (TOS)

The top of stack register is the accumulator of the MARC4. All arithmetic/logic, memory reference and I/O operations use this register. The TOS register gets the data from the ALU, the program memory, the RAM or via the I/O bus.

- Condition Code Register (CCR)

The 4-bit wide condition code register contains the branch, the carry and the interrupt enable flag. These bits indicates the current state of the CPU. The CCR flags are set or reset by ALU operations. The instructions SET_BCF, TOG_BF, CCR! and DI allow a direct manipulation of the condition code register.

Carry/Borrow (C)

The carry/borrow flag indicates that borrow or carry out of arithmetic logic unit (ALU) occurred during the last arithmetic operation. During shift and rotate operations this bit is used as a fifth bit. Boolean operations have no affect on the C flag.

Branch (B)

The branch flag controls the conditional program branching. When the branch flag was set by one of the previous instructions a conditional branch is taken. This flag is affected by arithmetic, logic, shift, and rotate operations.

Interrupt Enable (I)

The interrupt enable flag enables or disables the interrupt processing on a global basis. After reset or by executing the DI instruction the interrupt enable flag is reset and all interrupts are disabled. The µC does not process further interrupt requests until the interrupt enable flag is set again by either executing an EI, RTI or SLEEP instruction.

1.2.4 ALU

The 4-bit ALU performs all the arithmetic, logical, shift and rotate operations with the top two elements of the expression stack (TOS and TOS-1) and returns its result to the TOS. The ALU operations affect the carry/borrow and branch flag in the condition code register (CCR).

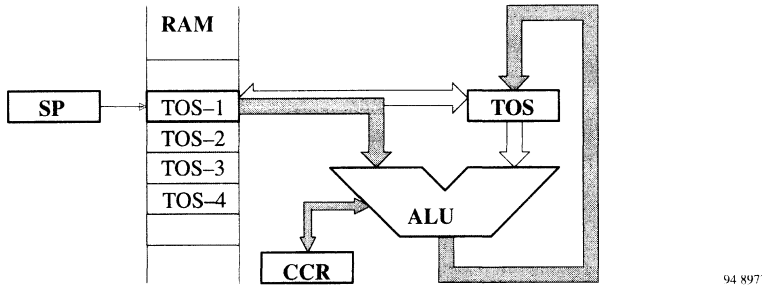


Figure 7. ALU zero address operations

1.2.5 Instruction Cycles

A MARC4 instruction word is one or two byte long and is executed within one or four machine-cycles. A machine–cycle consists of two system clocks (SYSCL). The MARC4 is a zero address machine. Most of the instructions are one byte long and are executed in only one machine–cycle. The CPU has an instruction pipeline, this allows the controller to fetch the next instruction from program memory at the same time as the present instruction is being executed. For more informations see section "MARC4 Instruction Set Overview".

1.2.6 I/O Bus

The I/O ports and the registers of the peripheral modules (timer 1, timer 2, EEPROM) are I/O mapped. The communication between the core and the on-chip peripherals takes place via the I/O bus and the associated I/O control bus. These buses are used for different functions: for read and write accesses, for the interrupt generation, to reset peripherals and for the SLEEP mode. With the MARC4 IN-instruction and OUT-instructions the I/O bus allows a direct read or write access to one of the 16 I/O addresses. More about the I/O access to the on-chip peripherals is described in the section "Peripheral modules".

The I/O buses are internal buses and are not accessible by the customer on the final microcontroller device, but they are used as the interface for the MARC4 emulation (see also the section "Emulation").

1.2.7 Interrupt Structure

The MARC4 can handle interrupts with eight different priority levels. They can be generated from the internal and external interrupt sources or by a software interrupt from the CPU itself. Each interrupt level has a hard-wired priority and an associated vector for the service routine in the ROM (see table 2). The programmer can enable or disable interrupts all together by setting or resetting the interrupt enable flag (I) in the CCR.

Interrupt processing

For processing the eight interrupt levels the MARC4 contains an interrupt controller with the 8-bit wide interrupt pending and interrupt active register. The interrupt controller samples all interrupt requests during every non-I/O instruction cycle and latches them in the interrupt pending register. If no higher priority interrupt is present in the interrupt active register it signals the CPU to interrupt the current program execution. If the interrupt enable bit is set the processor enters an interrupt acknowledge cycle. During this cycle a SHORT CALL instruction to the service routine is executed and the current PC is saved on the return stack. An interrupt service routine is finished with the RTI instruction. This instruction sets the interrupt enable flag, resets the corresponding bits in the interrupt pending/active register and fetches the return address from the return stack to the program counter. When the interrupt enable flag is reset (interrupts are disabled), the execution of interrupts is inhibited but not the logging of the interrupt requests in the interrupt pending register. The execution of the interrupt will be delayed until the interrupt enable flag is set again. But note that interrupts are lost if an interrupt request occurs during the corresponding bit in the pending register is still set. After the reset (power-on, external or watchdog reset), the interrupt enable flag and the interrupt pending and interrupt active register are reset.

Interrupt latency

The interrupt latency is the time from the falling edge of the interrupt to the interrupt service routine being activated. In the MARC4 this takes between 3 to 5 machine cycles depending on the state of the core.

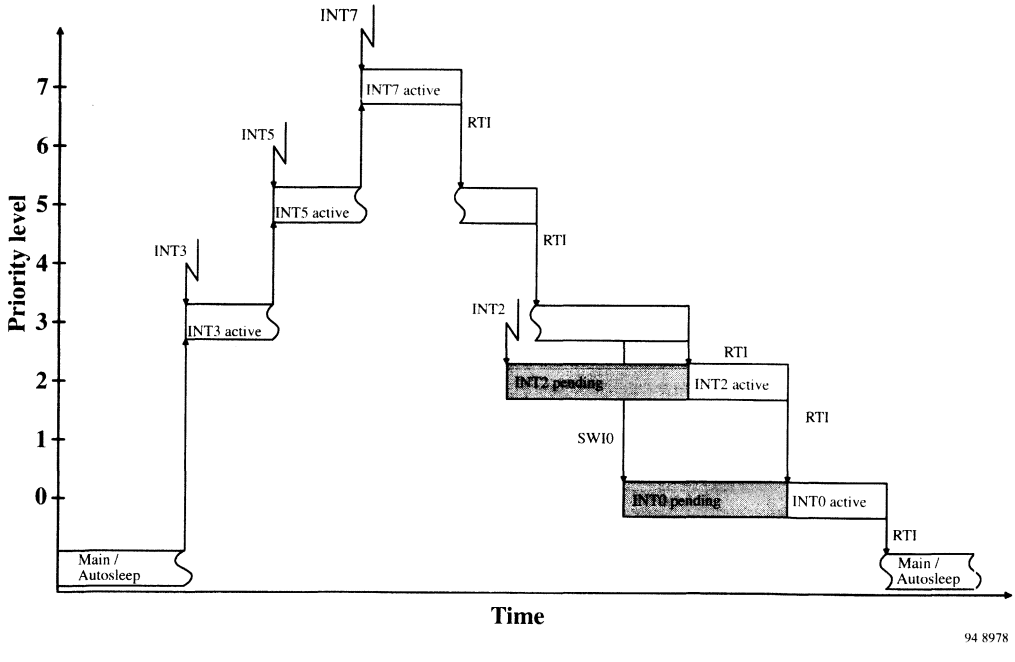


Figure 8. Interrupt handling

Table 2. Interrupt priority table

Interrupt	Priority	Vector Address	Interrupt Opcode (Acknowledge)	Function
INT0	lowest	040h	C8h (SCALL 040h)	Software interrupt (SWI0)
INT1		080h	D0h (SCALL 080h)	EEPROM write ready
INT2		0C0h	D8h (SCALL 0C0h)	External hardware interrupt, neg. edge at BP30 or BP31
INT3		100h	E0h (SCALL 100h)	External hardware interrupt, neg. edge at BP32 or BP33
INT4		140h	E8h (SCALL 140h)	Timer 1 interrupt
INT5		180h	F0h (SCALL 180h)	Timer 2 interrupt
INT6		1C0h	F8h (SCALL 1C0h)	External hardware interrupt, neg. edge at IP40 pin
INT7	highest	1E0h	FCh (SCALL 1E0h)	Software interrupt (SWI7)

Software Interrupts

The programmer can generate interrupts using the software interrupt instruction (SWI) which is supported in qFORTH by predefined macros named SWI0 to SWI7. The software triggered interrupt operates exactly like any hardware triggered interrupt. The SWI instruction takes the top two elements from the expression stack and writes the corresponding bits via the I/O bus to the interrupt pending register. Thus using the SWI instruction, interrupts can be re-prioritized or lower priority processes scheduled for later execution.

Hardware Interrupts

In the M44C260 are eleven hardware interrupt sources with six different levels. Each of these sources can be enabled or disabled separately with an interrupt mask bit in the IMR1 or IMR2 register.

Table 3. Hardware interrupts

Interrupt	Priority	Mask		Interrupt Source
		Register	Bit	
EEPROM write ready	INT1	EMS	IMEP	EEPROM end of write cycle
External interrupt port 3 (BP30 OR BP31)	INT2	IMR1	IM30	Negative edge at BP30
			IM31	Negative edge at BP31
External interrupt port 3 (BP32 OR BP33)	INT3	IMR1	IM32	Negative edge at BP32
			IM33	Negative edge at BP33
Timer 1 interrupt	INT4	IMR2	IMT1	Timer 1
Timer 2 interrupt	INT5	T2IC	IMAS	Timer A end of space/underflow
			IMAP	Timer A end of pulse/capture
			IMBS	Timer B end of space/underflow
			IMBP	Timer B end of pulse/capture
Ext. interrupt IP40 input	INT6	IMR2	IM6	Negative edge at IP40 input

1.3 Reset

The reset puts the CPU into a well-defined condition. The reset can be triggered by switching on the supply voltage, by a break-down of the supply voltage, by the watchdog timer or by pulling the NRST pad to low.

After any reset the branch-, carry- and interrupt enable flag in the Condition Code Register (CCR) , the interrupt pending register and the interrupt active register are reset. During the reset-cycle the I/O bus control signals are set to 'reset mode' thereby initializing all on-chip peripherals.

A reset is finished with a short call instruction (opcode C1h) to the program memory address 008h. This activates the initialization routine $RESET. With that routine the stack pointers, variables in the RAM and the peripheral must be initialized.

Power-on Reset

The power-on reset ensures that the core is activated not before the operating supply voltage has been reached.

A reset is also generated when the supply voltage remains below the operating range for more than 5 ms.

External Reset (NRST)

An external reset can be triggered with the NRST pin. For the external reset the pin should be low for a minimum of two machine cycles.

Watchdog Timer Reset

If the watchdog timer function of Timer 1 is enabled a reset is triggered with every watchdog counter overflow. To suppress that the watchdog counter must be reset by an access to the CWD-register (see also Timer 1/watchdog counter).

The power-on reset and watchdog reset are indicated in the same way as an external reset on the NRST pad.

1.4 Clock Generation

The M48C260 has two oscillators, one RC oscillator for the system clock generation and an additional 32-kHz crystal oscillator. The system clock generator provides the core and Timer 2 with the clock. The system clock frequency of the M48C260 is programmable for 1 or 2 MHz. The crystal oscillator is used as an exact time base for Timer 1. If no exact timing is required, the controller does not need an external crystal. In this case Timer 1 is provided with the system clock.

The configuration for both oscillators is programmable with the clock status control register (CSC), which is a subport register located in port CSUB. The required configuration has to be initialized after reset in the $RESET routine. The default setting after a reset is 1 MHz system clock and an active 32-kHz crystal oscillator.

After power-on or a SLEEP instruction the clock generator needs a start-up time until it runs with an exact timing. The CRDY bit in the CSC register indicates the start-up phase.

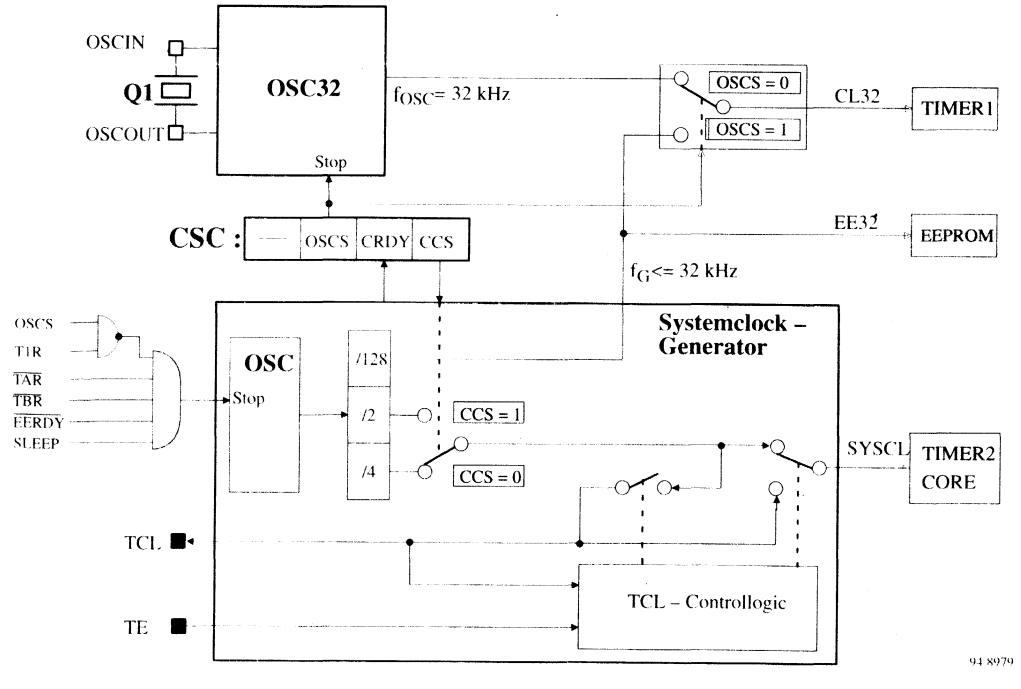


Figure 9. Clock module

1.4.1 Clock Status/Control Register (CSC)

Address: Ch Subaddress: 2h

	Bit 3	Bit 2	Bit 1	Bit 0
CSC	—	OSCS	CRDY	CCS

Reset value: X000h

OSCS **Oscillator Stop**
When OSCS = 0 the controller is configured to run with the 32-kHz crystal oscillator for Timer 1.
When OSCS = 1 the 32-kHz oscillator stops. For µC operation without crystal, this bit must be set after reset. In that case Timer 1 is provided from the internal RC oscillator.

CRDY **Clock Ready (status bit)**
CRDY = 0 indicates the start-up time of the oscillators.
CRDY = 1 indicates that the clock is ready. The µC runs with an exact timing.

CCS **Core Clock Select**
CCS = 0 selects 1 MHz system clock (SYSCL/TCL)
CCS = 1 selects 2 MHz system clock (SYSCL/TCL)

1.4.2 TCL Signal

The TCL pin can be used as input to supply the controller with an external clock. For this configuration the TCL pin must be held low for at least 0.5 ms during the reset cycle. The controller is working with clock frequencies up to 2.5 MHz. It is also possible to use the TCL pin as output to supply peripherals with the system clock. In this case the TE pin must be connected to V_{DD} level and the TCL pin must have a high impedance load.

1.5 Power Down Modes

The sleep mode is a shutdown condition which is used to reduce the average system power consumption in applications where the µC is not fully utilized. In this mode the system clock is stopped. The sleep mode is entered with the SLEEP instruction. This instruction sets the interrupt enable bit (I) in the condition code register to enable all interrupts and stops the core. During the sleep mode the peripheral modules remain active and are able to generate interrupts. The µC exits the sleep mode with any interrupt or a reset.

The sleep mode can only be kept when none of the interrupt pending or active register bits are set. The application of the $AUTOSLEEP routine ensures the correct function of the sleep mode.

The total power consumption is directly proportional to the active time of the µC. For a rough estimation of the expected average system current consumption, the following formula should be used:

$$I_{total}(V_{DD}, f_{Osc}) = I_{Sleep} + (I_{DD} * T_{active}/T_{total})$$

I_{DD} depends on V_{DD} and f_{Osc}.

Systemclock Generator Stop

The M48C260 has different power down modes. When the MARC4 core enters the sleep mode and no on-chip peripheral needs a clock signal (SYSCL) the system clock oscillator is stopped. Therefor the programmer should stop timer 1 and timer 2 during the sleep mode if they are not required. If the 32-kHz oscillator is not used it should be stopped. Under this condition the power consumption is extremely low (see following table).

Table 4. Power consumption at different power down modes

Mode	CPU-Core	TIMER 1 [T1R] TIMER 2 [TAR, TBR] EEPROM [EERDY]	RC Osc.	32-kHz-Osc. [OSCS]	Power-Consumption [µA]
1	SLEEP	T1R=0 AND TAR=0 AND TBR=0 AND EERDY=1	STOP	STOP	< 1.0
2	SLEEP	T1R=X, TAR=0 AND TBR=0 AND EERDY=1	STOP	RUN	< 1.0
3	SLEEP	T1R=1 OR TAR=1 OR TBR=1 OR EERDY=0	RUN	STOP	< x
4	SLEEP	T1R=X, TAR=1 OR TBR=1 OR EERDY=0	RUN	RUN	< x
5	RUN	T1R=X, TAR=X, TBR=X, EERDY=X	RUN	STOP	< y
6	RUN	T1R=X, TAR=X, TBR=X, EERDY=X	RUN	RUN	< y

2 Peripheral Modules

2.1 Addressing Peripherals

The access to the peripheral modules (ports, registers) is executed via the I/O bus. The IN- or OUT-instruction allows the direct addressing of 16 I/O ports. For the peripherals with a large number of registers, extended addressing is used. With two I/O operations an extended I/O port allows the access to 16 subports. The first OUT-instruction writes the subport address to the subaddress register, the second IN- or OUT-instruction reads data from or writes data to the addressed subport.

Table 5. I/O-addressing

I/O Operation	qFORTH Instructions	Description
Port 0, 1, 2, 3, 4, T2SC, EMS		
I/O read	port IN	Read data from port
I/O write	data port OUT	Write data to port
T2SUB, CSUB		
Extended I/O read	subaddress port OUT	Write subaddress to port
	port IN	Read data from subaddress
Extended I/O write	subaddress port OUT	Write subaddress to port
	data port OUT	Write data to subaddress
Extended I/O short read	port IN	Read data from current subaddress
ESUB		
Extended I/O read (byte)	subaddress port OUT	Write subaddress to port
	port IN	Read data high nibble from subaddress
	port IN	Read data low nibble from subaddress
Extended I/O write (byte)	subaddress port OUT	Write subaddress to port
	data port OUT	Write data low nibble to subaddress
	data port OUT	Write data high nibble to subaddress

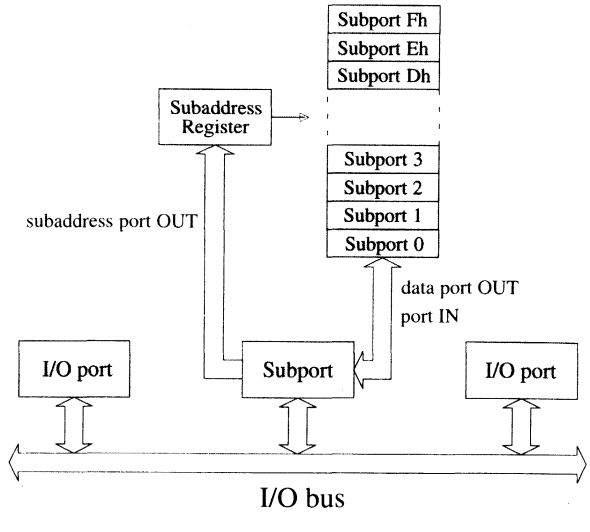


Figure 10. Extended I/O addressing

Table 6. Peripheral addresses

Addr.	Name	Function			
0	Port 0	Bidirectional port			
1	Port 1	Bidirectional port			
2	Port 2	Bidirectional port			
3	Port 3	Bidirectional port			
4	Port 4	Input port			
5	—				
6	—				
7	—				
8	T2SC	Timer 2 status and control register			
9	T2SUB	Subport for timer 2	Sub-address	Name	Register
			0	TARCH	Timer 2A space reload/capture register, high nibble
			1	TARCL	Timer 2A space reload/capture register, low nibble
			2	TARH	Timer 2A pulse reload register
			3	TARL	Timer 2A pulse reload register
			4	TBRCH	Timer 2B space reload/capture register, high nibble
			5	TBRCL	Timer 2B space reload/capture register, low nibble
			6	TBRH	Timer 2B pulse reload register
			7	TBRL	Timer 2B pulse reload register
			8	TAM1	Timer 2A mode register 1
			9	TAM2	Timer 2A mode register 2
			A	TBM1	Timer 2B mode register 1
			B	TBM2	Timer 2B mode register 2
			C	T2IC	Timer 2 interrupt control
			D	T2PC	Timer 2 prescaler control
			E	—	
			F	—	
A	EMS	EEPROM status register			
B	ESUB	Subport for EEPROM	Row 0 – Row F		
C	CSUB	Subport for watchdog, timer 1, interrupt masks, and clock generator	Sub-address	Name	Register
			0	WDC	Watchdog control register
			1	CWD	Clear watchdog counter
			2	CSC	Clock status/control register
			3	—	
			4	T1C	Timer 1 control register
			5	IMR1	Interrupt mask register 1
			6	IMR2	Interrupt mask register 2
			7-F	—	
D	—				
E	—				
F	—				

2.1.1 Input Port 4

Port 4 is the input port for the pins IP40, IP43, TA and TB. IP40 is also the interrupt input for INT6, and TA and TB are normally used for timer I/O functions.

	Bit 3	Bit 2	Bit 1	Bit 0
Input port 4	**IP43**	**TB/IP42**	**TA/IP41**	**IP40/INT6**

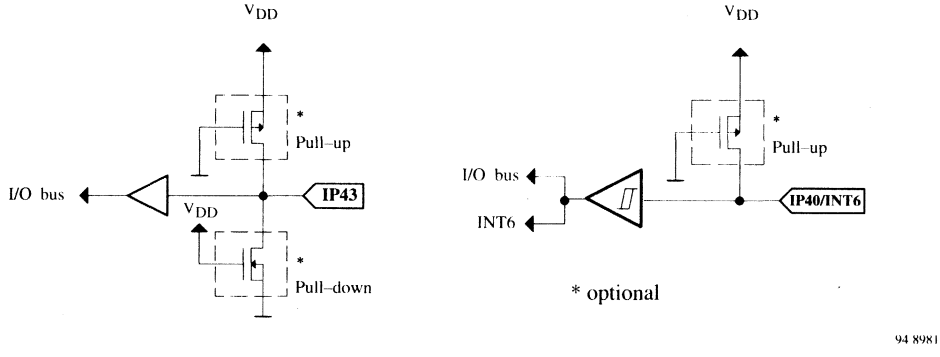


Figure 11. Input port IP40, IP43

2.1.2 Bidirectional Ports

Ports 0, 1, 2 and 3 are bidirectional 4-bit wide ports and may be used for data input or output. The data direction is programmable for a complete port only. The port is switched to output with an OUT-instruction and to input with an IN-instruction. The data written to a port will be stored into the output latches and appears immediately after the OUT-instruction at the port pin. After RESET all output latches are set to Fh and the ports are switched to input mode.

Note: Care must be taken when switching bidirectional ports from output to input. The capacitive load at this port may cause the data read to be the same as the last data written to this port. To avoid this, when switching the direction one of the following approaches should be used.

- Use two IN-instructions and DROP the first data nibble read. The first IN switches the port from output to input, DROP removes the first invalid nibble and the second IN reads the valid nibble.
- Use an OUT-instruction followed by an IN-instruction. With the OUT-instruction the capacitive load is charged or discharged depending on the optional pull-up /pull-down configuration. Write a "1" for pins with pull-up resistors and a "0" for pins with pull-down resistors.

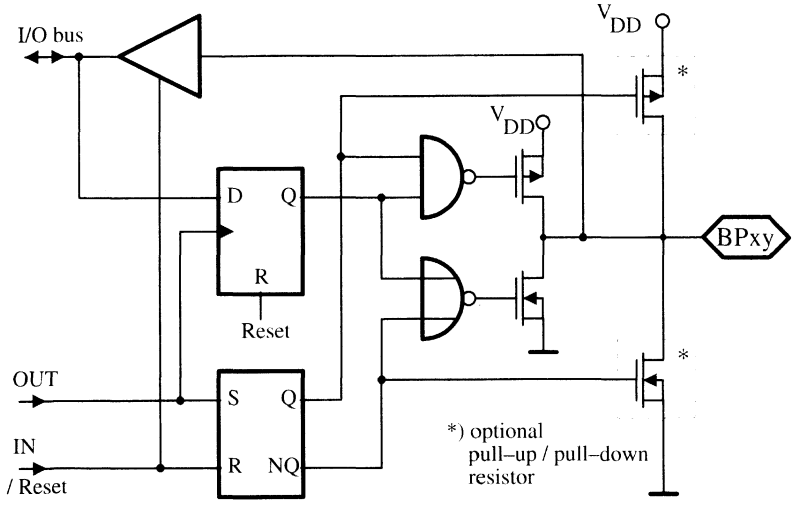


Figure 12. Bidirectional port

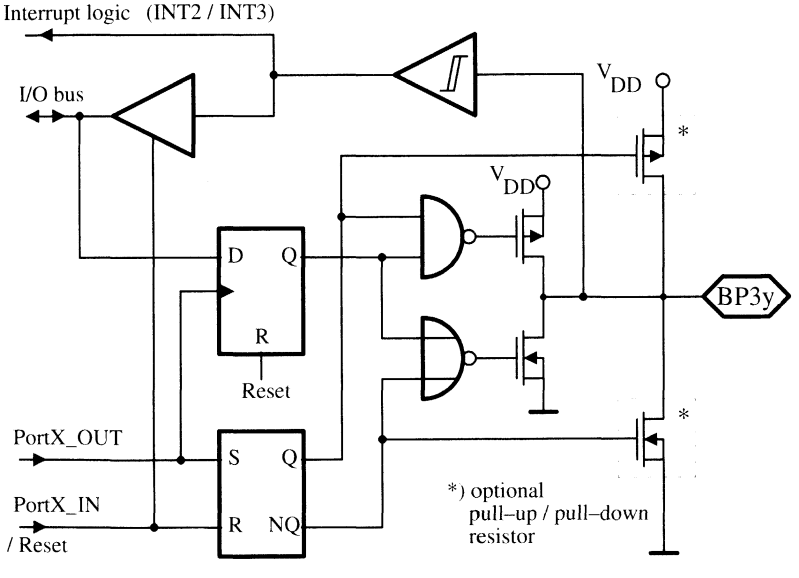


Figure 13. Bidirectional port 3 with interrupt input

2.1.3 External Interrupt Inputs

The pins IP40 and BP30 – BP33 can be used as external interrupt inputs. IP40 is used for INT6, BP32 and BP33 are used for INT3, and BP30 and BP31 are used for INT2. Pin IP40 is also used as an input port and BP30 – BP33 as a bidirectional port (see figure 11). Each of these external interrupt sources can be enabled or disabled with individually interrupt mask bits. A negative transition at one of these inputs requests an interrupt, when the corresponding mask bit is set. The interrupt masks are placed in the subport registers IMR1 and IMR2 of port CSUB.

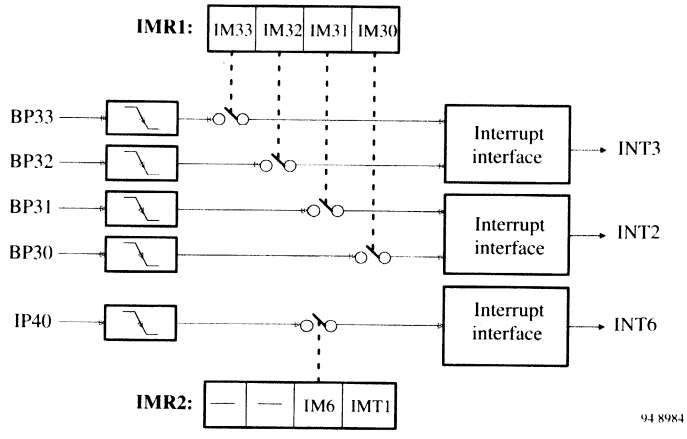


Figure 14. External interrupt inputs

2.2 Timer 1

Timer 1 is an interval timer for generating interrupts. Additional to the timer can be used as watchdog timer. The timer consists of a programmable 18 stage divider which is supplied with a 32-kHz clock and a 3-bit counter for the watchdog function (see figure 15). The time interval for a timer 1 interrupt (INT4) can be programmed with the timer control register from 1 ms up to 8.0 s. The timer 1 interrupt is maskable with the IMT1 bit.

The time interval for a watchdog reset can be programmed with the watchdog control register for 0.5, 2.0, 8.0 or 16.0 s. When the watchdog is active (WDR = 1, T1R = 1) the controller is reset with the overflow of the 3-bit watchdog counter. The application software has to ensure that the watchdog counter is reset by a write access to the CWD port before it overflows. Because the watchdog timer is supplied by the interval timer it is necessary that timer 1 is set active (T1R = 1).

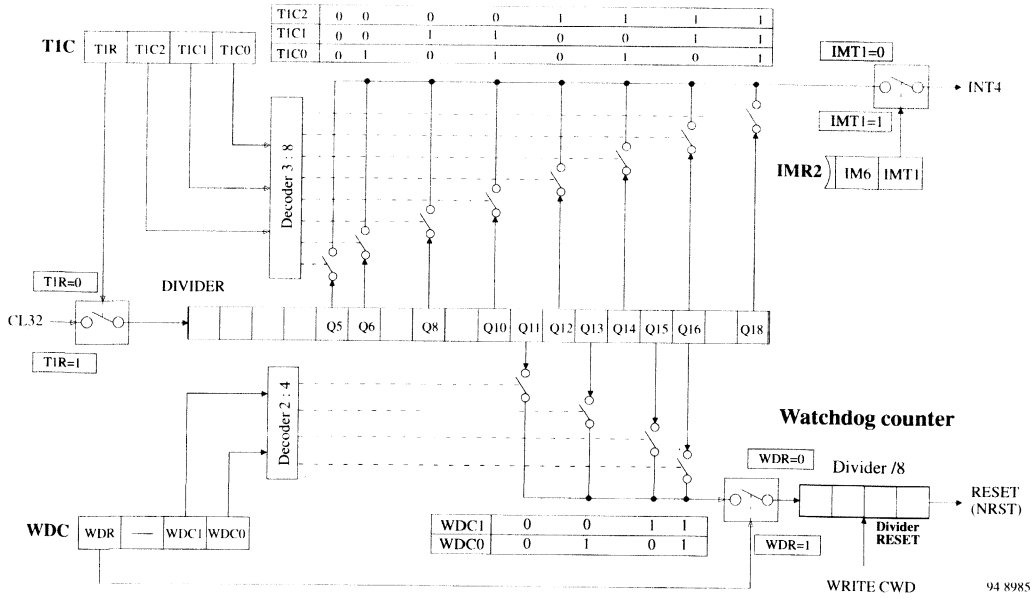


Figure 15. Timer 1

Timer 1 register

The registers of Timer 1 are I/O-mapped. They are subport register of port CSUB the access is made by extended I/O operations. The interval timer is controlled by the prescaler control register T1C. The interrupt mask IMT1 is placed in the interrupt mask register IMR2. The watchdog timer is controlled by the watchdog control register WDC and port CWD. A write access to CWD resets the watchdog counter.

2.2.1 T1C – Timer 1 Control Register

Address: 'C'h Subaddress 4

	Bit 3	2	1	0	
T1C	**T1R**	**T1C2**	**T1C1**	**T1C0**	**Reset value: 0000b**

T1R Timer 1 run
T1R = 0 stops the interval timer
T1R = 1 starts the interval timer

T1C2 Timer 1 control bit 2

T1C1 Timer 1 control bit 1

T1C0 Timer 1 control bit 0

This both bits select the time interval for a Timer 1 interrupt.

T1C2	T1C1	T1C0	Divider	Time Interval
0	0	0	32	0.9765625 ms
0	0	1	64	1.953125 ms
0	1	0	256	7.8125 ms
0	1	1	1024	31.25 ms
1	0	0	4096	125 ms
1	0	1	16384	500 ms
1	1	0	65536	2 s
1	1	1	262144	8 s

2.2.2 WDC – Watchdog Control Register

Address: 'C'h Subaddress 0

	Bit 3	2	1	0	
WDC	**WDR**	**—**	**WDM1**	**WDM0**	**Reset value: 0x00b**

WDR Watchdog run
WDR = 0 the watchdog counter is inactive and reset
WDR = 1 the watchdog counter is active and able to generate a reset when Timer 1 is running

WDC1 Watchdog mode 1

WDC0 Watchdog mode 0

This both bits control the time interval for the watchdog reset.

WDM 1	WDM 0	Divider	Delay time to Reset (s)
0	0	2048	0.5
0	1	8192	2
1	0	32768	8
1	1	524288	16

2.3 Timer 2

Timer 2 consists of the two timer/counter blocks Timer A and Timer B. Each block has one 8-bit downcounter and a programmable prescaler. The clock inputs can be programmed to count the system clocks, Timer A clocks or external clocks. The maximum clock rate for external clocks is the half system clock frequency (SYSCL/2). Each counter has a reload register for the pulse time and a reload register for the space time. Every counter underflow toggles the output and reloads the downcounter alternately from the pulse reload register or from the space reload register. This allows the generation of any duty cycles.

Addition both counters have a capture mode. In this mode an external signal or the Counter B output causes the current counter value to be captured into the corresponding capture register.

The timer has two I/O pins, TA for Timer A and TB for Timer B. Used as output the pins have a high level during the pulse time and a low level during the space time of the timer. As input the pins are used for the external counter clock or the capture signal. The inputs have a programmable edge detection to select the active edge of an external clock or capture signal.

Interrupts can be generated when a counter underflow or a capture event occurs. The interrupt function for timer 2 can be programmed with the interrupt control register. Both counter blocks share one interrupt vector (INT5).

Timer 2 Modes

There are various timer/counter modes for both blocks of Timer 2. They can be used separately or combined. The timer modes can be programmed with the timer control and mode registers.

Single Timer Modes

- **8-bit timer**
  Counter A/B is supplied by the system clock and is used to generate timer interrupts.
- **Pulse width modulation**
  Counter A/B is supplied by the system clock. The TA/TB pin is used as counter output. The duty cycle can be programmed with the pulse and space reload register.
- **Capture mode**
  Counter A/B is supplied by the system clock. The TA/TB pin is used as input. An external signal at the input causes the current counter value to be captured into the capture register.
- **Event counter**
  Counter A/B counts external clocks at the TA/TB pin. The capture register contains the current counter value and can be read.

Combined Timer Modes

- **16-bit timer**
  Counter A is supplied system clock and its output is coupled with the input of Counter B. In this mode the counter is used to generate timer interrupts.
- **16 bit capture mode**
  Counter A is supplied with the system clock and Counter B with the output of Counter A. An external signal at the TA pin causes the current counter value will be captured into the capture registers.
- **16-bit event counter**
  The output of Counter A is coupled with the input of Counter B to count external clocks at TA. The capture register of both counters contain the current counter values.
- **Burst generator**
  Counter A is supplied the system clock and its output is coupled with the input of Counter B. The output of Counter B controls the output signal of Counter A at the TA pin. The TA output is enabled during the pulse and disabled during the space of Counter B.
- **Event counter with time gate**
  Counter A counts the clocks at the TA pin and Counter B is supplied with the system clock. Each underflow of Counter B causes the counter value of Counter A to be captured into its capture register.

Timer 2 Register

All timer register are I/O mapped. The access to the Timer 2 status control register (T2SC) can be done with a direct I/O operation to T2SC. The status is read with an IN operation and a command to control the timer is written with an OUT operation. The remaining registers of Timer 2 are subport registers of port T2SUB. The access to those registers needs an extended I/O operation. The timer function can be configured with the mode registers TAM1, TAM2, TBM1, TBM2 and the interrupt control register T2IC. The timing depends on the contents of the prescaler control register T2PC and the reload registers. The capture registers are used to read the counter value.

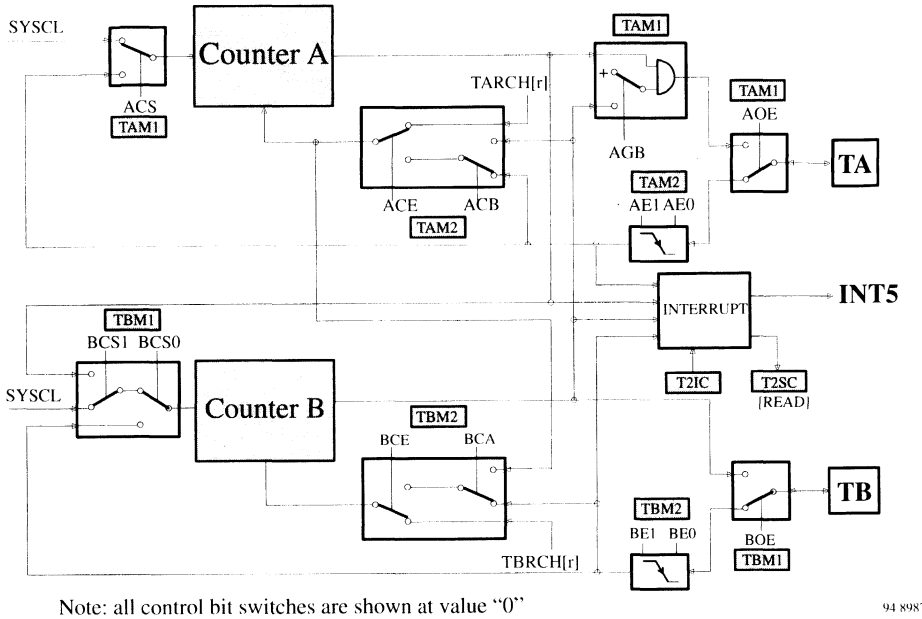


Figure 16. Timer 2

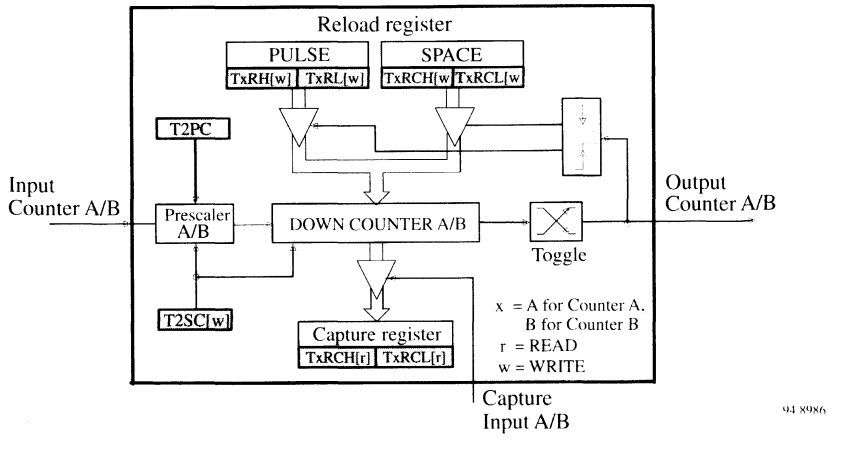


Figure 17. Counter A/B

2.3.1 Timer 2 Status/Control Register (T2SC)

Address: 8

Control register	Bit 3	2	1	0	
Write (T2SC)	**TBM**	**TAM**	**TBR**	**TAR**	**Reset value: 0000b**
Status register					
Read (T2SC)	**TBSU**	**TBPC**	**TASU**	**TAPC**	**Reset value: 0000b**

TAM, TAR: Timer A control bits to start or stop Timer A.

TBM, TBR: Timer B control bits to start or stop Timer B.

TBM	TAM	TBR	TAR	Timer 2 Commands
1	0	x	0	STOP_A
1	0	x	1	RUN_A
0	1	0	x	STOP_B
0	1	1	x	RUN_B
0	0	0	0	STOP_AB
0	0	1	1	RUN_AB
0	0	0	1	RUN_A-STOP_B
0	0	1	0	STOP_A-RUN_B
1	1	x	x	NOP

A STOP command resets the prescaler and counter.

A RUN command starts the counter with the next clock taking the value from the pulse reload register.

TBSU: Timer B end of space/underflow status bit.
When BCE* = 0 this bit will be set at the end of space time of Counter B.
When BCE = 1 this bit will be set with every Counter B underflow.

TBPC: Timer B end of pulse/capture status bit.
When BCE = 0 this bit will be set at the end of pulse time of Counter B.
When BCE = 1 this bit will be set when a capture event for Counter B occurs.

TASU: Timer A end of space/underflow status bit.
When ACE* = 0 this bit will be set at the end of space time of Counter A.
When ACE = 1 this bit will be set with each Counter A underflow.

TAPC: Timer A end of pulse/capture status bit.
When ACE = 0 this bit will be set at the end of pulse time of Counter A.
When ACE = 1 this bit will be set when a capture event for Counter A occurs.

*) ACE and BCE are the capture enable control bits in the timer mode registers TAM2 and TBM2.

The status bits TASU, TAPC, TBSU, TBPC will be reset after a READ access to T2SC!

2.3.2 Timer 2 Subport (T2SUB)

Address: 9

Table 7. Timer 2 subports

Subaddr.	Name	Meaning		Bit 3	Bit 2	Bit 1	Bit 0
0	TARCH [w]*	Timer A reload high		High-nibble			
	TARCH [r]*	Timer A capture high					
1	TARCL [w]*	Timer A reload low		Low-nibble			
	TARCL [r]*	Timer A capture low					
2	TARH	Timer A reload high		High-nibble			
3	TARL	Timer A reload low		Low-nibble			
4	TBRCH [w]*	Timer B reload high		High-nibble			
	TBRCH [r]*	Timer B capture high					
5	TBRCL [w]*	Timer B reload low		Low-nibble			
	TBRCL [r]*	Timer B capture low					
6	TBRH	Timer B reload high		High-nibble			
7	TBRL	Timer B reload low		Low-nibble			
8	TAM1	Timer A mode register 1		—	AGB	ACS	AOE
9	TAM2	Timer A mode register 2		ACB	ACE	AE1	AE0
A	TBM1	Timer B mode register 1		—	BCS1	BCS0	BOE
B	TBM2	Timer B mode register 2		BCA	BCE	BE1	BE0
C	T2IC	Timer 2 interrupt control		IMBS	IMBP	IMAS	IMAP
D	T2PC	Timer 2 prescaler control		BPC1	BPC0	APC1	APC0
E	—			—	—	—	—
F	—			—	—	—	—

* [w] write only, [r] read only

2.3.3 Timer 2 Reload Register

The 8–bit wide reload registers of Timer A and B are used to program the pulse and space width of the counter output signal.

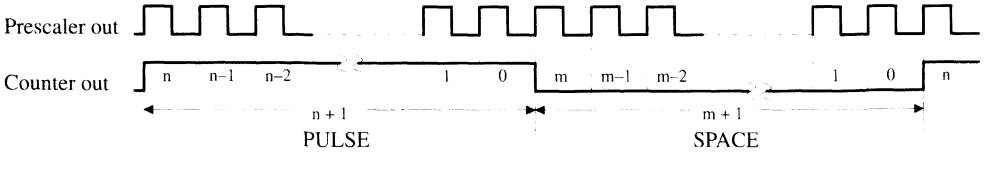
The first clock after a start command loads the downcounter with the value (n) from the pulse reload register and sets the counter output to 1. The downcounter decrements with each following clock and each underflow reloads alternately the value (m) from the space reload register or the value (n) from the pulse reload register and toggles the counter output.

The pulse and space width can be calculated as following:

Pulse time: Pulse = (n+1) x prescaler clocks

Spacetime: Space = (m+1) x prescaler clocks

$0 \leq m, n \leq 255$



Timer 2 Space Reload Register

The space reload register of Timer 2 is programmed by two write accesses to the subport addresses TARCH and TARCL or TBRCH and TBRCL of the Timer 2 subport T2SUB. The value (m) in the space reload register determines the space width. At the end of pulse the downcounter reloads the 8–bit value from the space reload register with the next clock of the prescaler output.

Space width: Space = (m+1) prescaler clocks
$0 \leq m \leq 255$

Timer 2 Pulse Reload Register

The pulse reload register of Timer 2 is programmed by two write accesses to the subport addresses TERH and TARL or TBRH and TBRL of the Timer 2 subport T2SUB. The value (n) in the pulse reload register determines the space width. At the end of space the downcounter reloads the 8–bit value from the pulse reload register with the next clock of the prescaler output.

Pulse width: Pulse = (n+1) prescaler clocks
$0 \leq n \leq 255$

2.3.4 Timer 2 Capture Register

The capture register is used to capture the current downcounter value when a capture event occurs. The value is kept in the capture register until the next capture event and can be read independent of the state of the downcounter. The capture events are programmable with the timer mode registers TAM2 and TBM2.

The capture registers are also used to read the counter value when the external capture mode is disabled. In this case the 8–bit counter value is transferred into the capture register by reading the high nibble TARCH or TBRCH. If the 16–bit event counter mode is enabled the complete 16–bit value is captured by reading first the high nibble TARCH of Timer A. This mechanism ensures the coherence of the counter high and low nibble during the read access.

2.3.5 Timer A Mode Register 1 (TAM1)

Address: 9 – Subaddress: 8

	Bit 3	2	1	0
TAM1	—	**AGB**	**ACS**	**AOE**

Reset value: 0000b

AGB Counter **A** output gated by Counter **B** output
AGB = 1 enables the burst generation mode. The output of Timer A is enabled during the pulse time of the Counter B and disabled (TA= 0) during the space time of the Counter B.

ACS Counter **A** clock select
This bit selects the source of the Counter A clock. When ACS = 0 the timer is supplied with internal SYSCL. When ACS = 1 the timer is supplied with an external clock on TA pin.

AOE Timer **A** output enable
AOE = 0 disables the counter output TA.
AOE = 1 enables the counter output TA.

2.3.6 Timer A Mode Register 2 (TAM2)

Address: 9 – Subaddress: 9

	Bit 3	2	1	0
TAM2	**ACB**	**ACE**	**AE1**	**AE0**

Reset Value: 0000b

ACB Timer **A** captured by Timer **B**
Selects the capture source for Timer A. When ACB = 0 the signal at the TA pin is used to generate a capture event. When ACB = 1 each transition at the Counter B output is used to generate a capture event for Timer A.

ACE Timer **A** capture enable
ACE = 1 enables the capture mode for Counter A. The occurrence of a capture event causes that the current downcounter value is loaded into the capture register.

AE1 Timer **A** edge select bit **1**

AE0 Timer **A** edge select bit **0**
Whit these bits the active edge for the counter clocks and capture signal is selected.

AE1	AE0	Active Edge for Counter Clock/Capture Events
0	0	positive edge at TA pin
0	1	negative edge at TA pin
1	0	first positive edge after timer start and then each transition at TA pin
1	1	first negative edge after timer start and then each transition at TA pin

2.3.7 Timer B Mode Register 1 (TBM1)

Address: 9 – Subaddress: Ah

	Bit 3	2	1	0
TBM1	**—**	**BCS1**	**BCS0**	**BOE**

Reset value: 0000b

BCS1 Timer **B** clock select bit **1**

BCS0 Timer **B** clock select bit **0**

These bits select the source of Counter B clock.

BCS1	BCS0	Counter B Input Signal
0	0	System clock (SYSCL)
1	0	Output signal of Counter A
x	1	External input signal at TB

BOE Timer **B** output enable
BOE = 0 disables the counter output TB.
BOE = 1 enables the counter output TB.

2.3.8 Timer B Mode Register 2 (TBM2)

Address: 9 – Subaddress: Bh

	Bit 3	2	1	0
TBM2	**BCA**	**BCE**	**BE1**	**BE0**

Reset value: 0000b

BCA Timer B is captured with Timer A capture signal. With BCA = 1 the external capture signal for Timer A is used to capture Timer B
simultaneously with Timer A.
Note: It is possible to capture Counter B by a read access to TARCH

BCE Timer **B** capture enable
BCE = 1 enables the capture mode for Counter B. A capture event loads the current downcounter value into the capture register.

BE1 Timer **B** edge select bit **1**

BE0 Timer **A** edge select bit **0**
With these bits the active edge for the counter clocks and capture signal is selected.

BE1	BE0	Active Edge for Clock/Capture Events
0	0	positive edge on TB pin
0	1	negative edge on TB pin
1	0	first positive edge after start timer and then each transition on TB pin
1	1	first negative edge after start timer and then each transition on TB pin

2.3.9 Timer 2 Prescaler Control Register (T2PC)

Address: 9 – Subaddress: Dh

	Bit 3	2	1	0	
T2PC	BPC1	BPC0	APC1	APC0	Reset Value: 0000b

BPC1 Timer **B** prescaler control bit **1**

BPC0 Timer **B** prescaler control bit **0**
These bits determine the divider for the prescaler of Timer B.

APC1 Timer **A** prescaler control bit **1**

APC0 Timer **A** prescaler control bit **0**
These bits determine the divider for the prescaler of Timer A.

BPC1/APC1	BPC0/APC0	Divider
0	0	1
0	1	4
1	0	16
1	1	64

2.3.10 Timer 2 Interrupt Control Register (T2IC)

Address: 9 – Subaddress: Ch

	Bit 3	2	1	0	
T2IC	IMBS	IMBP	IMAS	IMAP	Reset value: 0000b

IMBS Interrupt mask Timer B end of space/underflow
IMBS = 1 enables an INT5 interrupt, if BCE* = 0 at the end of space of Counter B, or if BCE = 1 at each Counter B underflow.

IMBP Interrupt mask Timer B end of pulse/capture
IMBP = 1 enables an INT5 interrupt, if BCE = 0 at the end of pulse of Counter B, or if BCE = 1 with a capture event for Counter B.

IMAS Interrupt mask Timer A end of space/underflow
IMAS = 1 enables an INT5 interrupt, if ACE* = 0 at the end of space of Counter A, or if ACE = 1 at each Counter A underflow.

IMAP Interrupt mask Timer A end of pulse/capture
IMAP = 1 enables an INT5 interrupt, if ACE = 0 at the end of pulse of Counter A, or if ACE = 1 with a capture event for Counter A.

Each interrupt source can be enabled or disabled individually by setting the corresponding maskbit.

*) ACE and BCE are the capture enable control bits in the timer mode registers TAM2 and TBM2.

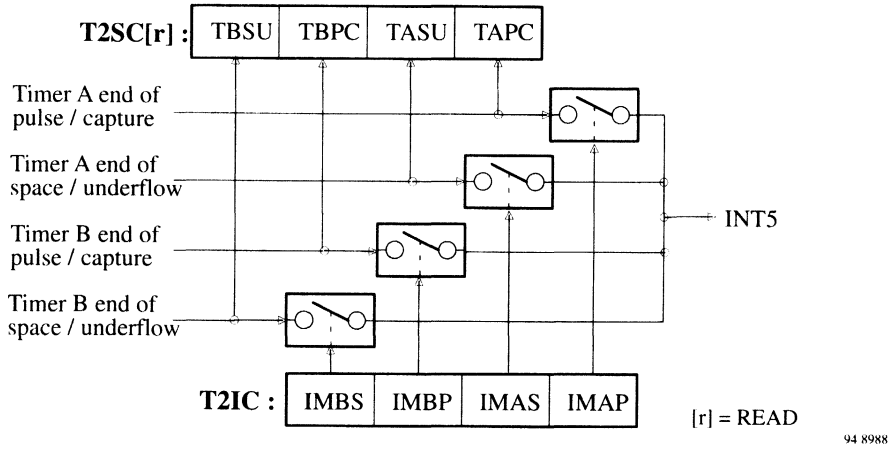


Figure 18. Timer 2 interrupt mask register

2.3.11 Timer I/O (TA/TB)

The timer I/O pins TA and TB are used as input for the external clock or capture signal and as output for the counter. The mode is controlled with AOE and BOE control bit. When AOE/BOE = 0 the pin is switched to input mode, when AOE/BOE = 1 the pin is switched to output mode. The pins also can be read with an IN-instruction via port 4 (TA with IP41 and TB with IP42).

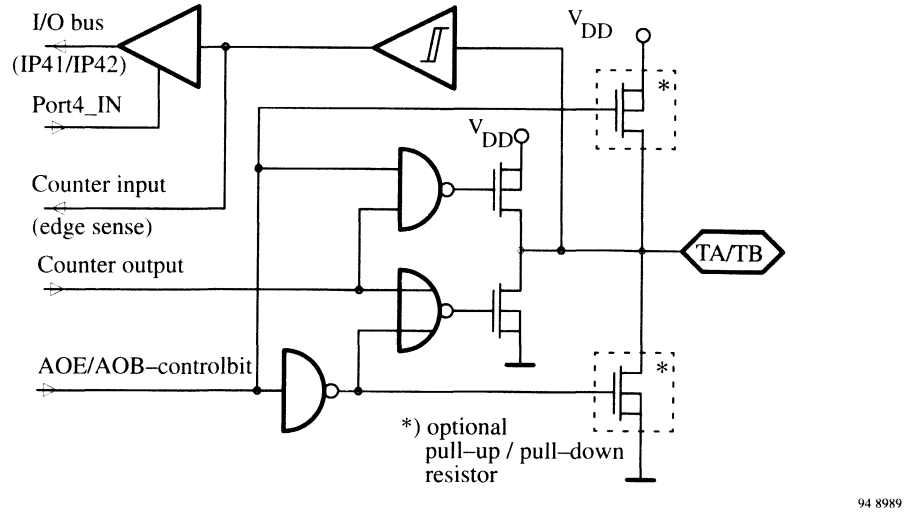


Figure 19. Timer I/O (TA/TB)

2.4 EEPROM

The EEPROM of the M48C260 is 128 bit wide and organized as an array of 16*8-bit. The EEPROM rows are I/O mapped and are subports of port ESUB. The access to any 8-bit row of the EEPROM is done by an extended 8-bit I/O operation or by special postincrement access. The EEPROM rows 12 to 15 can be write protected by hardware and software.

EEPROM SubPort (ESUB)
Address: Bh – Subaddress: 0-Fh

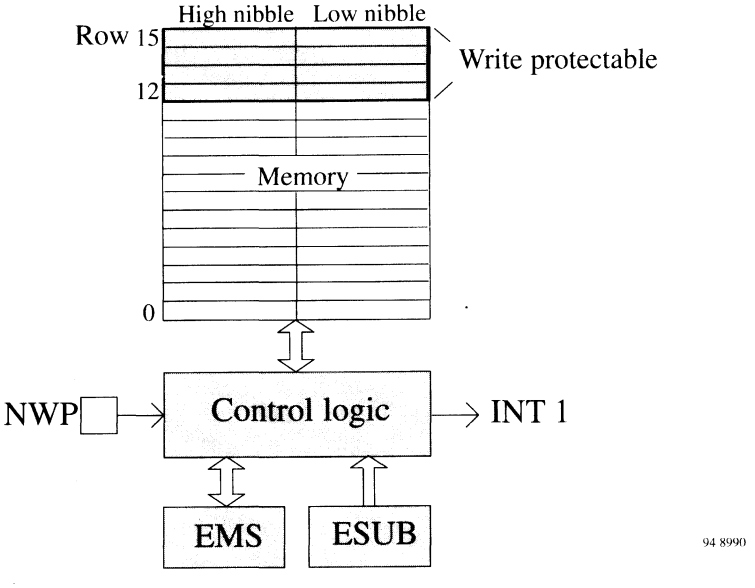


Figure 20. EEPROM

Read operation

A read operation needs an OUT- and two IN-instructions to port ESUB. First the the OUT operation writes the row address. The following two IN-instructions read the high nibble and then the low nibble of the addressed row.

qFORTH example:

Row address	ESUB OUT	(	—)
	EPSUB IN	(	—Data_High)
	EPSUB IN	(Data_High	— Data_High Data_Low)

Write operation

A write operation needs three OUT-instructions to port ESUB. The first operation writes the row address. The following two OUT-instructions write the low nibble and then the high nibble to the addressed row. After reset, rows 12 to 15 are write protected. To enable write operations to these rows the write enable bit (EWE) must be set. In all cases write accesses to these rows are disabled when pin NWP is low.

qFORTH example:

Row address	ESUB OUT	(Data_High Data_Low	— Data_High Data_Low)
	EPSUB OUT	(Data_High Data_Low	—Data_High)
	EPSUB OUT	(Data_High	—)

The internal EEPROM write cycle needs about 16 ms. During this cycle the EEPROM ready bit is reset (EPR = 0). After the data high nibble is written to the port ESUB the internal write cycle is started. During the internal write cycle (while EPR = 0), only read and write accesses to the EMS register are possible. All other EEPROM accesses have no effect.

Postincrement operations

The postincrement mode supports a fast access to consecutive EEPROM rows. A postincrement access is started by setting the EPI bit in the EEPROM mode register (EMS) followed by writing the row start address to port ESUB. After that the read or write operations to the consecutive EEPROM area, beginning at the start address, need only two IN- or OUT-instructions to read or write the data. The row address is incremented automatically after each complete row access (2 nibbles). A write access to the EEPROM mode register (EMS) terminates the postincrement mode.

Note: In the postincrement mode, it is not possible to change from read to write operations or vice versa before the current postincrement operation is finished.

Write ready interrupt (INT1)

At the end of the internal write cycle an interrupt is generated when the interrupt mask bit IMEP in the EEPROM mode register EMS is set. With this interrupt, successive write operations can be executed interrupt controlled within the INT1 interrupt service routine.

2.4.1 EEPROM Mode/Status Register (EMS)

Address: Ah

	Bit 3	2	1	0	
Mode register Write (EMS)	—	**EWE**	**EPI**	**IMEP**	Reset value: 0000b
Status register Read (EMS)	—	—	—	**EPR**	Reset value: xxx1b

EWE EEPROM write enable bit
EWE = 0 disables write accesses to rows 12-15
EWE = 1 enables write accesses to rows 12-15 when the NWP pin is high

EPI EEPROM postincrement mode enable
EPI = 1 activates a postincrement access after the next row address is written to port ESUB

IMEP Interrupt mask for EEPROM write ready interrupt
When IMEP is set an INT1 is generated with the end of the internal EEPROM write cycle

EPR EEPROM ready status flag
EPR = 0 indicates that the EEPROM is not ready for read or write operations (an internal write cycle is executed)
EPR = 1 indicates that the EEPROM is ready for read and write operations

After a write access to the EMS-Register postincrement operations are terminated and any incomplete EEPROM read and write sequence must be started again!

3 Appendix

3.1 Emulation

For emulation all MARC4 controllers have a special emulation mode. It is activated by setting the TE pin to logic HIGH level during reset. In this mode the internal CPU core is inactive and the I/O buses are available via port 0 and port 1 to allow the emulator the access to the on-chip peripherals. The emulator contains a special emulation CPU with a MARC4 core and additional breakpoint logic and takes over the core function. The basic function of the emulator is to evaluate the customer's program and hardware in real time. Thus permits the analysation of any timing, hardware or software problems the simulation of the application. For more informations about emulation see "Emulator Manual".

3.2 Programming the EEPROM Program Memory

Programming the 4K × 8-bit EEPROM program memory is done using a special PC–controlled programming device. Details on use of this device and the corresponding software are given in the Programming Device User Manual.

To start programming the data memory, the microcontroller is switched to a special I/O mode, where the core and all peripherals are set inactive and the two I/O buses are available via port 0 (data) and port 1 (control). Then the customer application data is transfered to the controller vio port 0 in blocks of 64 nibble size. Programming is started automatically after each block. The programming high voltage is generated on chip.

After programming the memory a verify run is started, where the just written data is read out and compared bit by bit to the original source file. This ensures that the contents of the ROM is error free.

3.3 MARC4 Instruction Set

The MARC4 instruction set is optimized for the high level programming language qFORTH. A lot of MARC4 instructions are qFORTH words. This enables the compiler to generate fast and compact program code. The MARC4 is a zero address machine with a compact and efficient instruction code. Most of the instructions are single byte instructions. This operations are performed and no source or destination address information. Only BRANCH, CALL and RAM access instructions need address informations and a length of two bytes for long address operations. In all there are five types of instruction formats with a length of one and two bytes.

Zero address operations like arithmetical, logical, shift and rotate operations are performed with data placed on the top of expression stack (TOS and TOS–1). Also I/O– and stack operations are single byte zero address operations and are performed with the top expression stack location.

A literal is a 4-bit constant value which is placed on the data stack. In the MARC4 native code they are represented as LIT_<value>, where <value> is the hexadecimal representation from 0 to 15 (0...F). This range is a result of the MARC4's 4-bit data width. The 6-bit short address and the 12-bit long address formats are both used to address the byte-wide ROM via CALL and conditional branch instructions. This results in a ROM address space of up to 4K*8-bit words.

The MARC4 instruction includes both short and long call instructions as well as conditional branch instructions. On execution the address part of the instructions word are directly loaded into the program counter. Long call and branch instructions can jump anywhere within the program memory area..The lower six bits from the short call (SCALL) and short branch (SBRA) instruction are handled in different way. The six bit SCALL address is multiplied by three and then loaded into the PC. This allows calls within the zero page (000 to 1FFh). The six bit SBRA address is loaded immediately into the lower six bits of the PC. This allows jumps within the 64 byte segment addressed by the upper six bits of the PC.

The CALL and SCALL instructions write the incremented program counter contents to the return stack. This address is loaded back to the PC when the associated EXIT or RTI instruction is encountered. The long RAM address format is used by the four 8-bit RAM address registers which can be pre-increment, post-decrement or loaded directly from the MARC4's internal bus. This results in a direct accessible RAM address space of up to 256 × 4-bit.

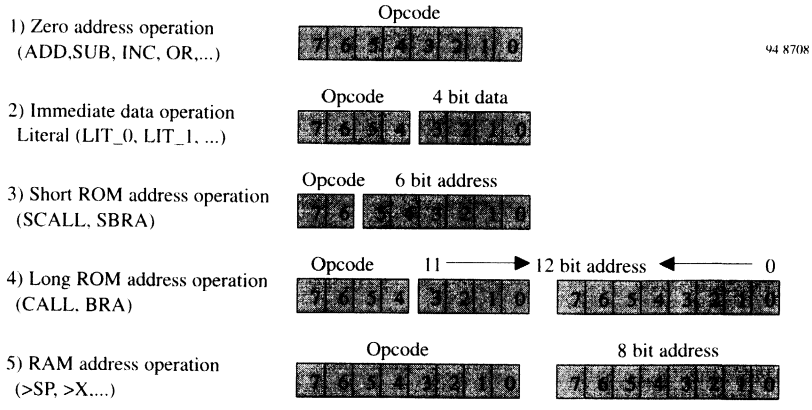


Figure 21. MARC4 opcode formats

3.3.1 MARC4 Instruction Set Overview

Mnemonic	Description	Cycles/ Bytes
	Arithmetic operations:	
ADD	Add	1/1
ADDC	Add with carry	1/1
SUB	Subtract	1/1
SUBB	Subtract with borrow	1/1
DAA	Decimal adjust	1/1
INC	Increment TOS	1/1
DEC	Decrement TOS	1/1
DECR	Decrement. 4-bit index on return stack	2/1
	Compare operations:	
CMP_EQ	Compare equal	1/1
CMP_NE	Compare not equal	1/1
CMP_LT	Compare less than	1/1
CMP_LE	Compare less equal	1/1
CMP_GT	Compare greater than	1/1
CMP_GE	Compare greater equal	1/1
	Logical operations:	
XOR	Exclusive OR	1/1
AND	AND	1/1
OR	OR	1/1
NOT	1's complement	1/1
SHL	Shift left into carry	1/1
SHR	Shift right into carry	1/1
ROL	Rotate left through carry	1/1
ROR	Rotate right through carry	1/1

Mnemonic	Description	Cycles/ Bytes
	Flag operations:	
TOG_BF	Toggle branch flag	1/1
SET_BFC	Set branch flag	1/1
DI	Disable all interrupts	1/1
CCR!	Store TOS into CCR	1/1
CCR@	Fetch CCR onto TOS	1/1
	Program branching:	
BRA $xxx	Conditional long branch	2/2
CALL $xxx	Long call (current page)	3/2
SBRA $xxx	Conditional short branch	2/1
SCALL$xxx	Short call (zero page)	2/1
EXIT	Return from subroutine	2/1
RTI	Return from interrupt	2/1
SWI	Software interrupt	1/1
SLEEP	Activate sleep mode	1/1
NOP	No operation	1/1
	Register operations:	
SP@	Fetch the current SP	2/1
RP@	Fetch the current RP	2/1
X@	Fetch the contents of X	2/1
Y@	Fetch the contents of Y	2/1
SP!	Move the top 2 into SP	2/1
RP!	Move the top 2 into RP	2/1
X!	Move the top 2 into X	2/1
Y!	Move the top 2 into Y	2/1
>SP $xx	Store direct address to SP	2/2
>RP $xx	Store direct address to RP	2/2
>X $xx	Store direct address into X	2/2
>Y $xx	Store direct address into Y	2/2

Mnemonic	Description	Cycles/ Bytes
	Stack operations:	
SWAP	Exchange the top 2 nibble	1/1
OVER	Copy TOS-1 to the top	1/1
DUP	Duplicate the top nibble	1/1
ROT	Move TOS-2 to the top	3/1
DROP	Remove the top nibble	1/1
>R	Move the top nibble onto the return stack	1/1
2>R	Move the top 2 nibble onto the return stack	3/1
3>R	Move the top 3 nibble onto the return stack	4/1
R@	Copy 1 nibble from the return stack	1/1
2R@	Copy 2 nibbles from the return stack	2/1
3R@	Copy 3 nibbles from the return stack	4/1
DROPR	Remove the top of return stack (12-Bit)	1/1
LIT_n	Push immediate value (1 nibble) onto TOS	1/1
	ROM data operations:	
TABLE	Fetch 8-bit constant from ROM	3

Mnemonic	Description	Cycles/ Bytes
	Memory operations:	
[X]@ [Y]@	Fetch 1 nibble from RAM indirect addressed by X- or Y-register	1/1
[+X]@ [+Y]@	Fetch 1 nibble from RAM indirect addr. by pre-increm. X- or Y-register	1/1
[X-]@ [Y-]@	Fetch 1 nibble from RAM indirect addr. by post-decrem. X- or Y-register	1/1
[>X]@ $xx [>Y]@ $xx	Fetch 1 nibble from RAM direct addressed by X- or Y-register	2/2
[X]! [Y]!	Store 1 nibble into RAM indirect addressed by [X]	1/1
[+X]! [+Y]!	Store 1 nibble into RAM indirect addressed by pre-incremented [X]	1/1
[X-]! [Y-]!	Store 1 nibble into RAM indirect addr. by post-decrem. X- or Y-register	1/1
[>X]! $xx [>Y]! $xx	Store 1 nibble into RAM direct addressed by X- or Y-register	2/2
	I/O operations:	
IN	Read I/O-Port onto TOS	1/1
OUT	Write TOS to I/O port	1/1

3.3.2 qFORTH Language Overview

MARC4 controller are programmed in the high level language qFORTH which is based upon the FORTH-83 language standard, the **qFORTH** compiler generates native code for a 4-bit FORTH-architecture single chip microcomputer, the TEMIC **MARC4**.**MARC4** applications are all programmed in **qFORTH** which is designed specifically for efficient real time control. Since the qFORTH compiler generates highly optimized code, there is no advantage or point in programming the **MARC4** in assembly code. The high level of code efficiency generated by the qFORTH compiler is achieved by the use of modern optimization techniques such as branch-instruction size minimization, fast procedure calls, pointer tracking and many peephole optimizations.

Langage features:

Expandability
Many of the fundamental qFORTH operations are directly implemented in the MARC4 instruction set.

Stack oriented
All operations communicate with one another via the data stack and use the reverse polish form of notation (RPN)

Structured programming
qFORTH supports structured programming

Reentrant
Different tasks can share the same code.

Recursive
qFORTH routines can call themselves.

Native code inclusion
In qFORTH there is no separation of high level constructs from the native code mnemonics.

3.4 The qFORTH language -Quick Reference Guide

3.4.1 Arithmetic/Logical

-	EXP (n1 n2 — n1-n2)	Subtract the top two values
+	EXP (n1 n2 — n1+n2)	Add up the two top 4-bit values
-C	EXP (n1 n2 — n1+/n+/C)	1's compl. subtract with borrow
+C	EXP (n1 n2 — n1+n2+C)	Add with carry top two values
1+	EXP (n — n+1)	Increment the top value by 1
1-	EXP (n — n–1)	Decrement the top value by 1
2*	EXP (n — n*2)	Multiply the top value by 2
2/	EXP (n — n DIV 2)	Divide the 4-bit top value by 2
D+	EXP (d1 d2 — d1+d2)	Add the top two 8-bit values
D-	EXP (d1 d2 — d1-d2)	Subtract the top two 8-bit values
D2/	EXP (d — d/2)	Divide the top 8-bit value by 2
D2*	EXP (d — d*2)	Multiply the top 8-bit value by 2
M+	EXP (d1 n — d2)	Add a 4-bit to an 8-bit value
M-	EXP (d1 n — d2)	Subtract 4-bit from an 8-bit value
AND	EXP (n1 n2 — n1^n2)	Bitwise AND of top two values
OR	EXP (n1 n2 — n1 v n2)	Bitwise OR the top two values
ROL	EXP (—)	Rotate TOS left through carry
ROR	EXP (—)	Rotate TOS right through carry
SHL	EXP (n — n*2)	Shift TOS value left into carry
SHR	EXP (n — n/2)	Shift TOS value right into carry
NEGATE	EXP (n — –n)	2's complement the TOS value
DNEGATE	EXP (d — –d)	2's complement top 8-bit value
NOT	EXP (n — /n)	1's complement of the top value
XOR	EXP (n1 n2 — n3)	Bitwise Ex-OR the top 2 values

3.4.2 Comparisons

>	EXP (n1 n2 —)	If n1>n2, then branch flag set
<	EXP (n1 n2 —)	If n1<n2, then branch flag set
>=	EXP (n1 n2 —)	If n1>=n2, then branch flag set
<=	EXP (n1 n2 —)	If n1<=n2, then branch flag set
<>	EXP (n1 n2 —)	If n1<>n2, then branch flag set
=	EXP (n1 n2 —)	If n1=n2, then branch flag set
0<>	EXP (n —)	If n <>0, then branch flag set
0=	EXP (n —)	If n = 0, then branch flag set
D>	EXP (d1 d2 —)	If d1>d2, then branch flag set
D<	EXP (d1 d2 —)	If d1<d2, then branch flag set
D>=	EXP (d1 d2 —)	If d1>=d2, then branch flag set
D<=	EXP (d1 d2 —)	If d1<=d2, then branch flag set
D=	EXP (d1 d2 —)	If d1=d2, then branch flag set
D<>	EXP (d1 d2 —)	If d1<>d2, then branch flag set
D0<>	EXP (d —)	If d <>0, then branch flag set
D0=	EXP (d —)	If d =0, then branch flag set
DMAX	EXP (d1 d2 — dMax)	8-bit maximum value of d1, d2
DMIN	EXP (d1 d2 — dMin)	8-bit minimum value of d1, d2
MAX	EXP (n1 n2 — nMax)	4-bit maximum value of n1, n2
MIN	EXP (n1 n2 — nMin)	4-bit minimum value of n1, n2

3.4.3 Control Structures

AGAIN	**EXP (—)**	Ends an infinite loop BEGIN .. AGAIN
BEGIN	**EXP (—)**	BEGIN of most control structures
CASE	**EXP (n — n)**	Begin of CASE .. ENDCASE block
DO	**EXP (limit start —)**	Initializes an iterative DO..LOOP
	RET (— ullimit|start)	
ELSE	**EXP (—)**	Executed when IF condition is false
ENDCASE	**EXP (n —)**	End of CASE..ENDCASE block
ENDOF	**EXP (n — n)**	End of <n> OF .. ENDOF block
EXECUTE	**EXP (ROMAddr —)**	Execute word located at ROMAddr
EXIT	**RET (ROMAddr —)**	Unstructured EXIT from ':'-definition
IF	**EXP (—)**	Conditional IF .. ELSE .. THEN block
LOOP	**EXP (—)**	Repeat LOOP, if index+1<limit
<n> OF	**EXP (c n —)**	Execute CASE block, if n =c
REPEAT	**EXP (—)**	Unconditional branch to BEGIN of BEGIN .. WHILE REPEAT
THEN	**EXP (—)**	Closes an IF statement
UNTIL	**EXP (—)**	Branch to BEGIN, if condition is false
WHILE	**EXP (—)**	Execute WHILE .. REPEAT block, if condition is true
+LOOP	**EXP (n —)**	Repeat LOOP, if I+n < limit
	RET (ullimit|I — ullimit|I+n)	
#DO	**EXP (n —) RET (— ululn)**	Execute the #DO .. #LOOP block n-times
#LOOP	**EXP (—)**	Decrement loop index by 1 downto zero
	RET (ulul|I—ulul|I-1)	
?DO	**EXP (Limit Start —)**	if start=limit, skip LOOP block
?LEAVE	**EXP (—)**	Exit any loop, if condition is true
-?LEAVE	**EXP (—)**	Exit any loop, if condition is false

3.4.4 Stack Operations

0 .. Fh,	**EXP (— n)**	
0 .. 15	**EXP (— n)**	Push 4-bit literal on EXP stack
' <name>	**EXP (— ROMAddr)**	Places ROM address of colon-definition <name> on EXP stack
<ROT	**EXP (n1 n2 n — n n1 n2)**	Move top value to 3rd stack pos.
>R	**EXP (n —) RET (— ululn)**	Move top value onto the return stack
?DUP	**EXP (n — n n)**	Duplicate top value, if n <>0
DEPTH	**EXP (— n)**	Get current expression stack depth
DROP	**EXP (n —)**	Remove the top 4-bit value
DUP	**EXP (n — n n)**	Duplicate the top 4-bit value
I	**EXP (— I) RET (ulul|I — ulul|I)**	Copy loop index I from return to expression stack
J	**EXP (— J)**	Fetch index value of outer loop [2nd return stack level entry]
	RET (ulul|J ulul|I — ulul|J ulul|I)	
NIP	**EXP (n1 n2 — n2)**	Drop second to top 4-bit value
OVER	**EXP (n1 n2 — n1 n2 n1)**	Copy 2nd over top 4-bit value
PICK	**EXP (x — n[x])**	Copy the x-th value from the expression stack onto TOS
RFREE	**EXP (— n)**	Get # of unused RET stack entries
R>	**EXP (— n) RET (ululn —)**	Move top 4-bits from return to expression stack
R@	**EXP (— n)**	Copy top 4-bits from return to expression stack
	RET (ululn — ululn)	
ROLL	**EXP (n —)**	Move n-th value within stack to top

ROT	**EXP (n1 n2 n — n2 n n1)**	Move 3rd stack value to top pos.
SWAP	**EXP (n1 n2 — n2 n1)**	Exchange top two values on stack
TUCK	**EXP (n1 n2 — n2 n1 n2)**	Duplicate top value, move under second item
2>R	**EXP (n1 n2 —)**	Move top two values from expression to return stack
	RET (— u|n2|n1)	
2DROP	**EXP (n1 n2 —)**	Drop top 2 values from the stack
2DUP	**EXP (d — d d)**	Duplicate top 8-bit value
2NIP	**EXP (d1 d2 — d2)**	Drop 2nd 8-bit value from stack
2OVER	**EXP (d1 d2 — d1 d2 d1)**	Copy 2nd 8-bit value over top value
2<ROT	**EXP (d1 d2 d — d d1 d2)**	Move top 8-bit value to 3rd pos'n
2R>	**EXP (— n1 n2)**	Move top 8-bits from return to expression stack
	RET (u|n2|n1 —)	
2R@	**EXP (— n1 n2)**	Copy top 8-bits from return to expression stack
	RET (u|n2|n1 — u|n2|n1)	
2ROT	**EXP (d1 d2 d — d2 d d1)**	Move 3rd 8-bit value to top value
2SWAP	**EXP (d1 d2 — d2 d1)**	Exchange top two 8-bit values
2TUCK	**EXP (d1 d2 — d2 d1 d2)**	Tuck top 8-bits under 2nd byte
3>R	**EXP (n1 n2 n3 —)**	Move top 3 nibbles from the expression onto
	RET (— n3|n2|n1)	the return stack
3DROP	**EXP (n1 n2 n3 —)**	Remove top 3 nibbles from stack
3DUP	**EXP (t — t t)**	Duplicate top 12-bit value
3R>	**EXP (— n1 n2 n3)**	Move top 3 nibbles from return to the expression stack
	RET (n3|n2|n1 —)	
3R@	**EXP (— n1 n2 n3)**	Copy 3 nibbles (1 entry) from the return
	RET (n3|n2|n1 — n3|n2|n1)	to the expression stack

3.4.5 Memory Operations

!	**EXP (n addr —)**	Store a 4-bit value in RAM
@	**EXP (addr — n)**	Fetch a 4-bit value from RAM
+!	**EXP (n addr —)**	Add 4-bit value to RAM contents
1+!	**EXP (addr —)**	Increment a 4-bit value in RAM
1–!	**EXP (addr —)**	Decrement a 4-bit value in RAM
2!	**EXP (d addr —)**	Store an 8-bit value in RAM
2@	**EXP (addr — d)**	Fetch an 8-bit value from RAM
D+!	**EXP (d addr —)**	Add 8-bit value to byte in RAM
D–!	**EXP (d addr —)**	Subtract 8-bit value from a byte in RAM
DTABLE@	**EXP (ROMAddr n — d)**	Indexed fetch of a ROM constant
DTOGGLE	**EXP (d addr —)**	Exclusive-OR 8-bit value with byte in RAM
ERASE	**EXP (addr n —)**	Sets n memory cells to 0
FILL	**EXP (addr n n1 —)**	Fill n memory cells with n1
MOVE	**EXP (n from to —)**	Move a n-digit array in memory
ROMByte@	**EXP (ROMAddr — d)**	Fetch an 8-bit ROM constant
TOGGLE	**EXP (n addr —)**	Ex-OR value at address with n
3!	**EXP (nh nm nl addr —)**	Store 12-bit value into a RAM array
3@	**EXP (addr — nh nm nl)**	Fetch 12-bit value from RAM
T+!	**EXP (nh nm nl addr —)**	Add 12-bits to 3 RAM cells
T–!	**EXP (nh nm nl addr —)**	Subtract 12-bits from 3 nibble RAM array
TD+!	**EXP (d addr —)**	Add byte to a 3 nibble RAM array
TD–!	**EXP (d addr —)**	Subtract byte from 3 nibble array

3.4.6 Predefined Structures

(ccccccc)		In-line comment definition
\ ccccccc		Comment until end of the line
: <name>	**RET (—)**	Begin of a colon definition
;	**RET (ROMAddr —)**	Exit; ends any colon definition
[FIRST]	**EXP (— 0)**	Index (=0) for first array element
[LAST]	**EXP (— nld)**	Index for last array element
CODE	**EXP (—)**	Begins an in-line macro definition
END-CODE	**EXP (—)**	Ends an In-line macro definition
ARRAY	**EXP (n —)**	Allocates space for a 4-bit array
2ARRAY	**EXP (n —)**	Allocates space for an 8-bit array
CONSTANT	**EXP (n —)**	Defines a 4-bit constant
2CONSTANT	**EXP (d —)**	Defines an 8-bit constant
LARRAY	**EXP (d —)**	Allocates space for a long 4-bit array with up to 255 elements
2LARRAY	**EXP (d —)**	Allocates space for a long byte array
Index	**EXP (nld addr—addr')**	Run-time array access using a variable array index
ROMCONST	**EXP (—)**	Define ROM look-up table with 8-bit values
VARIABLE	**EXP (—)**	Allocates memory for 4-bit value
2VARIABLE	**EXP (—)**	Creates an 8-bit variable
<n> ALLOT		Allocate space for <n+1> nibbles of un-initialized RAM
AT <address>		Fixed <address> placement
: INTx	**RET (— ROMAddr)**	Interrupt service routine entry
$AutoSleep		Entry point address on return stack underflow
: $RESET	**EXP (—)**	Entry point on power-on reset

3.4.7 Assembler Mnemonics

ADD	**EXP (n1 n2 — n1+n2)**	Add the top two 4-bit values
ADDC	**EXP (n1 n2 — n1+n2+C)**	Add with carry top two values
CCR!	**EXP (n —)**	Write top value into the CCR
CCR@	**EXP (— n)**	Fetch the CCR onto top of stack
CMP_EQ	**EXP (n1 n2 — n1)**	If n1=n2, then branch flag set
CMP_GE	**EXP (n1 n2 — n1)**	If n1>=n2, then branch flag set
CMP_GT	**EXP (n1 n2 — n1)**	If n1>n2, then branch flag set
CMP_LE	**EXP (n1 n2 — n1)**	If n1<=n2, then branch flag set
CMP_LT	**EXP (n1 n2 — n1)**	If n1<n2, then branch flag set
CMP_NE	**EXP (n1 n2 — n1)**	If n1<>n2, then branch flag set
CLR_BCF	**EXP (—)**	Clear branch and carry flag
SET_BCF	**EXP (—)**	Set branch and carry flag
TOG_BF	**EXP (—)**	Toggle the branch flag
DAA	**EXP (n>9 or C set — n+6)**	BCD arithmetic adjust [addition]
DAS	**EXP (n — 10+/n+C)**	9's complement for BCD subtract
DEC	**EXP (n — n–1)**	Decrement top value by 1
DECR	**RET (ululI — ululI–1)**	Decrement value on the return stack
DI	**EXP (—)**	Disable interrupts
DROPR	**RET (ululu —)**	Drop element from return stack
EXIT	**RET (ROMAddr —)**	Exit from current ':'-definition
EI	**EXP (—)**	Enable interrupts
IN	**EXP (port — data)**	Read data from an I/O port
INC	**EXP (n — n+1)**	Increment the top value by 1
NOP	**EXP (—)**	No operation
NOT	**EXP (n — /n)**	1's complement of the top value

RP!	**EXP (d —)**	Store as return stack pointer
RP@	**EXP (— d)**	Fetch current RET stack pointer
RTI	**RET (RETAddr —)**	Return from interrupt routine
SLEEP	**EXP (—)**	Enter 'sleep-mode', enable all interrupts
SWI0 SWI7	**EXP (—)**	Software triggered interrupt
SP!	**EXP (d —)**	Store as stack pointer
SP@	**EXP (— d)**	Fetch current stack pointer
SUB	**EXP (n1 n2 — n1-n2)**	2's complement subtraction
SUBB	**EXP (n1 n2 — n1+/n2+C)**	1's compl. subtract with borrow
TABLE	**EXP (— d)**	
	RET (RetAddr RomAddr —)	Fetches an 8-bit constant from an address in ROM
OUT	**EXP (data port —)**	Write data to I/O port
X@	**EXP (— d)**	Fetch current × register contents
[X]@	**EXP (— n)**	Indirect × fetch of RAM contents
[+X]@	**EXP (— n)**	Pre-incr. × indirect RAM fetch
[X–]@	**EXP (— n)**	Postdecr. × indirect RAM fetch
[>X]@ $xx	**EXP (— n)**	Direct RAM fetch, × addressed
X!	**EXP (d —)**	Move 8-bit address to × register
[X]!	**EXP (n —)**	Indirect × store of RAM contents
[+X]!	**EXP (n —)**	Pre-incr. × indirect RAM store
[X–]!	**EXP (n —)**	Postdecr. × indirect RAM store
[>X]! $xx	**EXP (n —)**	Direct RAM store, × addressed
Y@	**EXP (— d)**	Fetch current Y register contents
[Y]@	**EXP (— n)**	Indirect Y fetch of RAM contents
[+Y]@	**EXP (— n)**	Pre-incr. Y indirect RAM fetch
[Y–]@	**EXP (— n)**	Postdecr. Y indirect RAM fetch
[>Y]@ $xx	**EXP (— n)**	Direct RAM fetch, Y addressed
Y!	**EXP (d —)**	Move address to Y register
[Y]!	**EXP (n —)**	Indirect Y store of RAM contents
[+Y]!	**EXP (n —)**	Pre-incr. Y indirect RAM store
[Y–]!	**EXP (n —)**	Postdecr. Y indirect RAM store
[>Y]! $xx	**EXP (n —)**	Direct RAM store, Y addressed
>RP $xx	**EXP (—)**	Set return stack pointer
>SP $xx	**EXP (—)**	Set expression stack pointer
>X $xx	**EXP (—)**	Set × register immediate
>Y $xx	**EXP (—)**	Set Y register immediate

Notes:

RET (–)	Return address stack effects
EXP (–)	Expression (or data) stack effects
True condition	Means branch flag set in CCR
False condition	Means branch flag reset in CCR
n	4-bit data value
d	8-bit data value
addr	8-bit RAM address
ROMaddr	12-bit ROM address

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Voltages are given relative to V_{SS}.

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	– 0.3 to + 7.0	V
Input voltage (on any pin)	V_{IN}	V_{SS} –0.3 ≤ V_{IN} ≤ V_{DD} +0.3	V
Output short circuit duration	t_{short}	indefinite	sec
Operating temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	T_{stg}	–40 to +130	°C
Thermal resistance (PLCC)	R_{thJA}	110	K/W
Soldering temperature (t ≤ 10 s)	T_{sd}	260	°C

Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operational the device at any condition above those indicated in the operational section of these specification is not implied. Exposure to absolute maximum rating condition for an extended period may affect device reliability. All inputs and outputs are protected against high electrostatic voltages or electric fields. However, precautions to minimize built-up of electrostatic charges during handling are recommended. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., V_{DD}).

4.2 DC Operating Characteristics

Supply voltage V_{DD} = 2.4 to 6.2 V, V_{SS} = 0 V, T_{amb} = –40 to 85°C, unless otherwise specified

Parameters	Test Conditions / Pins		Symbol	Min.	Typ.	Max.	Unit
Power supply							
Active current (CPU active)	V_{DD} = 2.4 V	f_{SYSCL}=1MHz	I_{DD}			1.0	mA
		f_{SYSCL}=2MHz				2.0	mA
	V_{DD} = 6.2 V	f_{SYSCL}=1MHz				2.6	mA
		f_{SYSCL}=2MHz				5.2	mA
Power down current (CPU sleep, RC oscillator active)	V_{DD} = 2.4 V	f_{SYSCL}=1MHz	I_{PD}			0.4	mA
		f_{SYSCL}=2MHz				0.8	mA
	V_{DD} = 6.2 V	f_{SYSCL}=1MHz				0.6	mA
		f_{SYSCL}=2MHz				1.0	mA
Sleep current (CPU sleep, RC oscillator inactive)	V_{DD} = 2.4 V		I_{Sleep}			1.0	µA
	V_{DD} = 6.2 V					1.0	µA
Sleep current (CPU sleep, RC oscillator inactive)	V_{DD} = 2.4 V		I_{Sleep}			0.5	µA
	V_{DD} = 6.2 V					0.5	µA
	T_{amb} = 25°C						

Supply voltage V_{DD} = 2.4 to 6.2 V, V_{SS} = 0 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power-on reset threshold voltage: Note x figure xx						
POR threshold voltage		V_{POR}	1.5		2.1	V
POR hysteresis		ΔV_{POR}		100		mV
Schmitt-trigger input voltage: Pin INT6, TA, TB, port 40 and port 3						
Negative-going threshold voltage	V_{DD} = 2.4 to 6.2 V	V_{T-}	V_{SS}		0.3*V_{DD}	V
Positive-going threshold voltage	V_{DD} = 2.4 to 6.2 V	V_{T+}	0.7*V_{DD}		V_{DD}	V
Hysteresis (VT ± VT–)	V_{DD} = 2.4 to 6.2 V	V_H		0.1*V_{DD}		
Input voltage: Pin NRST, TE, NWP, TCL, and port 0, 1, 2, port 43:						
Input voltage LOW	V_{DD} = 2.4 to 6.2 V	V_{IL}	V_{SS}		0.2*V_{DD}	V
Input voltage HIGH	V_{DD} = 2.4 to 6.2 V	V_{IH}	0.8*V_{DD}		V_{DD}	V
Input current: Bidirectional ports 0, 1, 2, 3, input port 4 with pull-up resistor Pin NRST, TCL, INT6						
Input LOW current	V_{DD}= 2.4 V V_{IL}= V_{SS} V_{DD}= 6.2 V	I_{IL}	–2.7 –28	–6.7 –60	–13 –103	µA µA
Input current: Bidirectional ports 0, 1, 2, 3, input port 4 with pull-down resistor Pin TE, NWP, TA, TB						
Input HIGH current	V_{DD} = 2.4 V V_{IH} = V_{DD} V_{DD} = 6.2 V	I_{IH}	2.7 30	6.3 60	12 100	µA µA
Output current: Bidirectional ports 0, 1, 2, 3 and TA, TB						
Output LOW current	V_{DD} = 2.4 V V_{OL} = 0.2*V_{DD} V_{DD} = 6.2 V	I_{OL}	0.8 6	1.6 11	2.8 17	mA mA
Output HIGH current	V_{DD} = 2.4 V V_{OH} = 0.8*V_{DD} V_{DD} = 6.2 V	I_{OH}	–0.6 –4	–1.3 –7.5	–2.2 –12	mA mA
Output current: Pin TCL						
Output LOW current	V_{DD} = 2.4 V V_{OL} = 0.2*V_{DD} V_{DD} = 6.2 V	I_{OL}	1.6 12	3.2 22	5.6 34	mA mA
Output HIGH current	V_{DD} = 2.4 V V_{OH} = 0.8*V_{DD} V_{DD} = 6.2 V	I_{OH}	–1.2 –8	–2.6 –15	–4.4 –24	mA mA

4.3 AC Characteristics

Supply voltage V_{DD} = 2.4 to 6.2 V, V_{SS} = 0 V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Timer 2A and 2B input timing						
Timer input clock		f_{TI}			SYSCL	–
Timer input LOW time	Rise/fall time < 10 ns	t_{TIL}	50			ns
Timer input HIFG time	Rise/fall time < 10 ns	t_{TIH}	50			ns
Interrupt request input timing						
Int. request LOW time	Rise/fall time < 10 ns	t_{IRL}	50			ns
Int. request HIGH time	Rise/fall time < 10 ns	t_{IRH}	50			ns
TCL clock						
TCL input clock		f_{TCL}			2	MHz
TCL input LOW time		t_{TCLL}	250			ns
TCL input HIGH time		t_{TCLH}	0.250		10	µs
TCL rise time		t_{TCLR}				
TCL fall time		t_{TCLF}			10	ns
Reset timing						
Power-on reset time		T_{POR}		100	500	µs
NRES input LOW time		T_{POR}	4*SYSCL			µs
EEPROM write cycle						
EEPROM write time	Note 1	t_{EEW}		16		ms
EEPROM write cycles		n_W	$5*10^5$	10^6		–
Operation cycle time						
System clock cycle	CCS = 1 Note 1 CCS = 0	t_{SYSCL}		477 954		ns ns
RC oscillator						
Frequency	Note 1	f_{RC1}		1048		kHz
Stability	Note 1	$\Delta f/f$		2000		ppm
Stabilization time	Note 1	t_S		1000		s
32 kHz oscillator						
Frequency		f_X		32.768		kHz
Start up time		t_{SQ}				s
Stability	Note 2	$\Delta f/f$	–10		10	ppm
Integrated input/output capacitances		C_{IN} C_{OUT}		10		pF
External 32 kHz crystal parameters						
Crystal frequency		f_X		32.768		kHz
Series resistance		RS		30	50	kΩ
Static capacitance		C0		1.5		pF
Dynamic capacitance		C1		3		fF

Note 1: With connected crystal (pin 5, 6) and after start up time of crystal oscillator.

Note 2: Depend on the connected quartz crystal.

Crystal

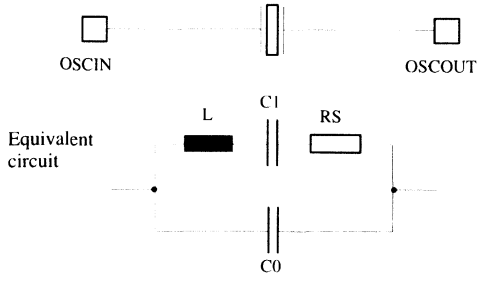


Figure 22. Equivalent crystal circuit

Power-on reset

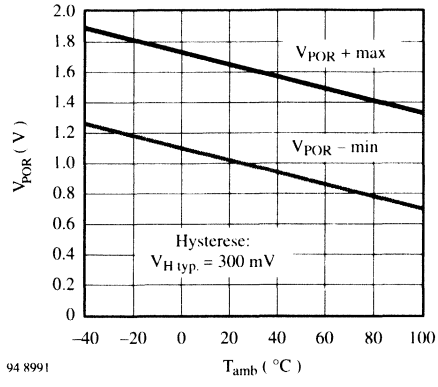


Figure 23. Thresholds for POR vs. ambient temperature

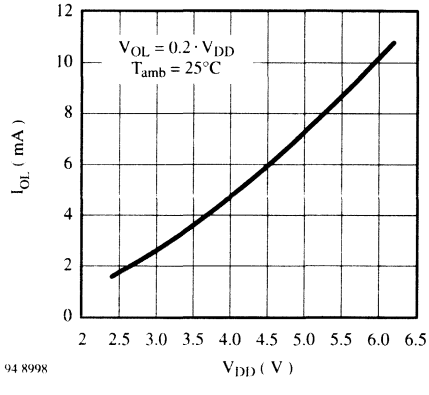


Figure 24. Output LOW current vs. supply voltage

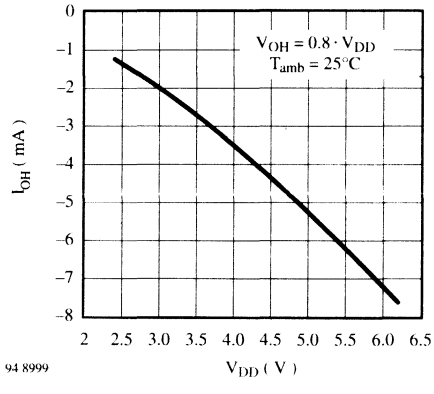


Figure 26. Output HIGH current vs. supply voltage

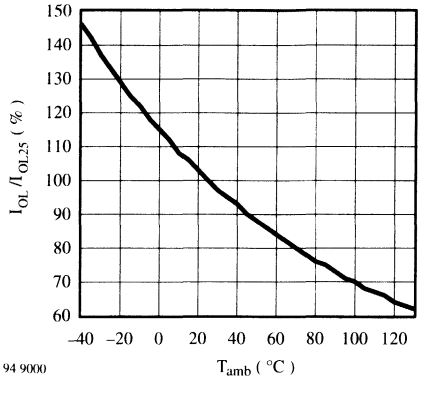


Figure 25. Output LOW current standardized to 25°C vs. temp.

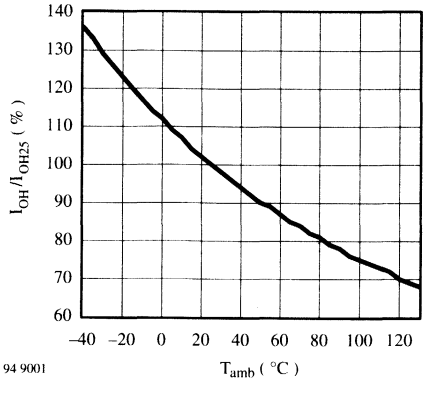


Figure 27. Output HIGH current standardized to 25°C vs temp.

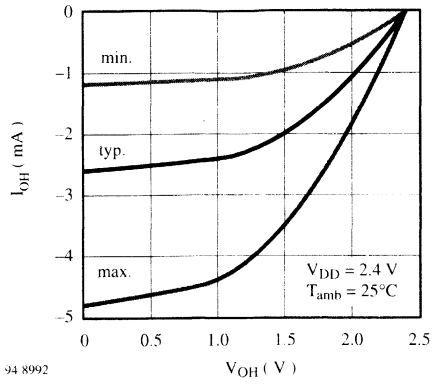


Figure 28. Output HIGH current vs. output HIGH voltage

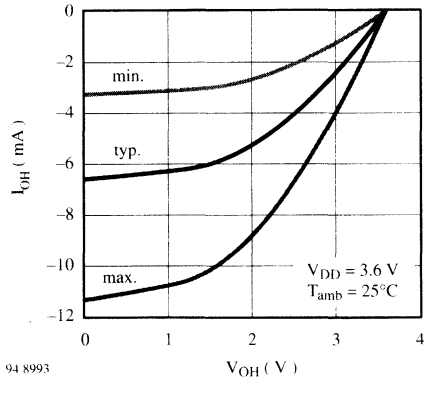


Figure 29. Output HIGH current vs. output HIGH voltage

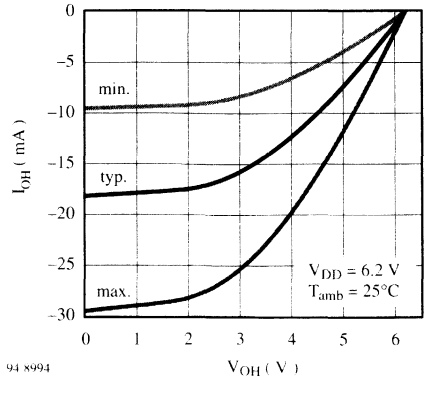


Figure 30. Output HIGH current vs. output HIGH voltage

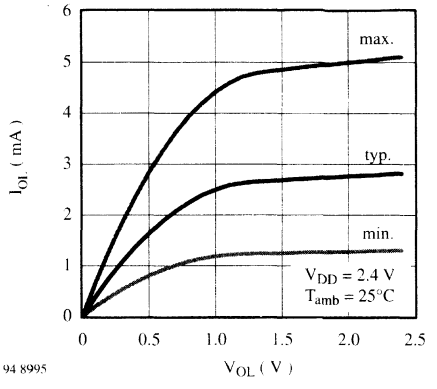


Figure 31. Output LOW current vs. output LOW voltage

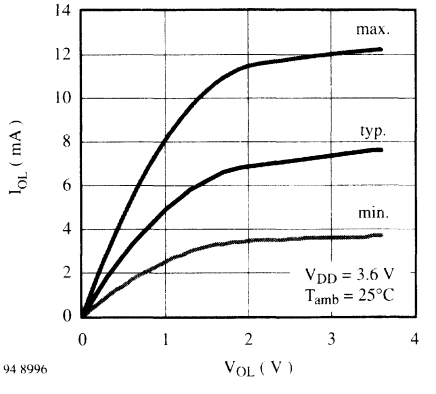


Figure 32. Output LOW current vs. output LOW voltage

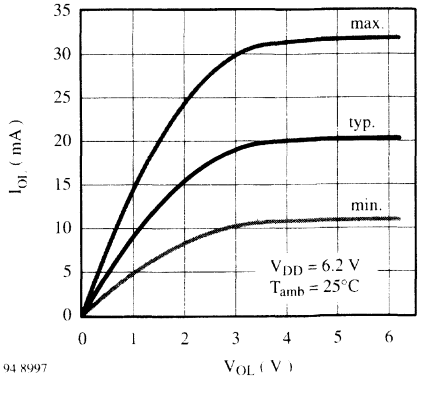


Figure 33. Output LOW current vs. output LOW voltage

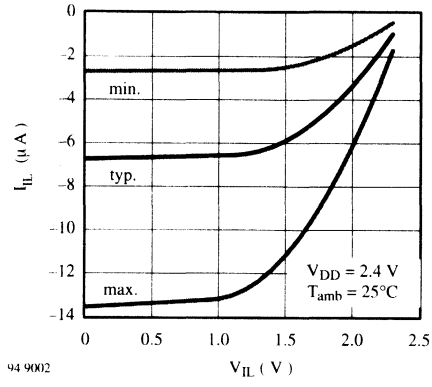


Figure 34. Input LOW current vs. input LOW voltage

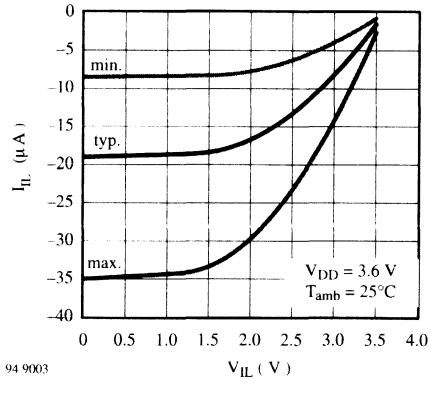


Figure 35. Input LOW current vs. input LOW voltage

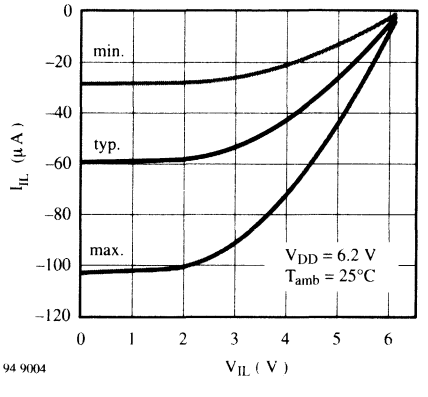


Figure 36. Input LOW current vs. input LOW voltage

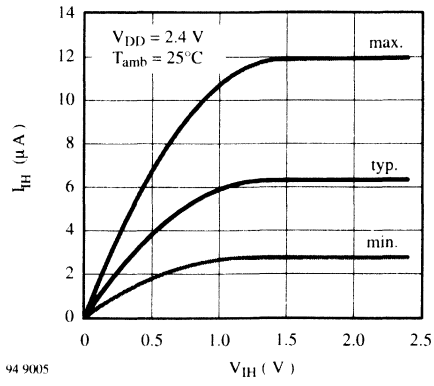


Figure 37. Input HIGH current vs. input HIGH voltage

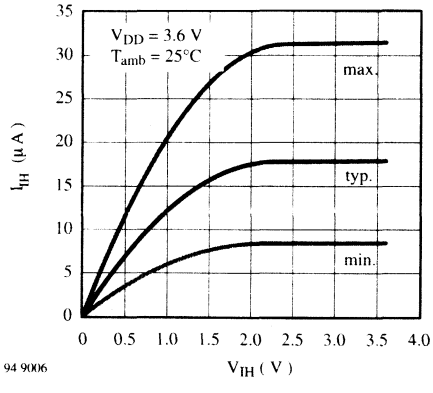


Figure 38. Input HIGH current vs. input HIGH voltage

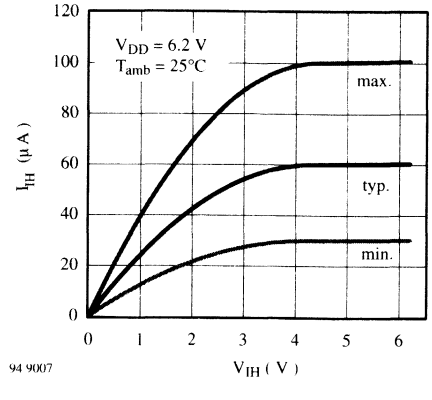


Figure 39. Input HIGH current vs. input HIGH voltage

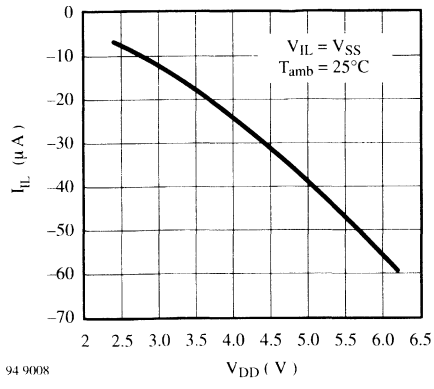


Figure 40. Input LOW current vs. supply voltage

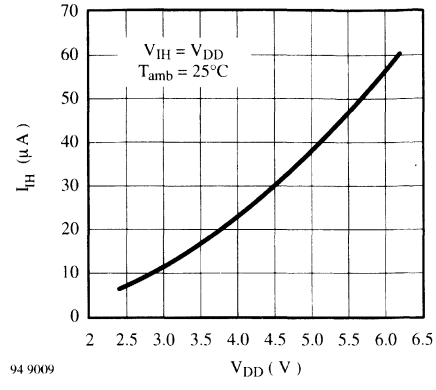


Figure 42. Input HIGH current vs. supply voltage

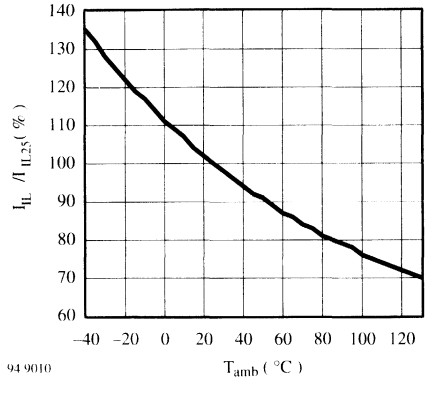


Figure 41. Input LOW current standardized to 25°C vs. temperature

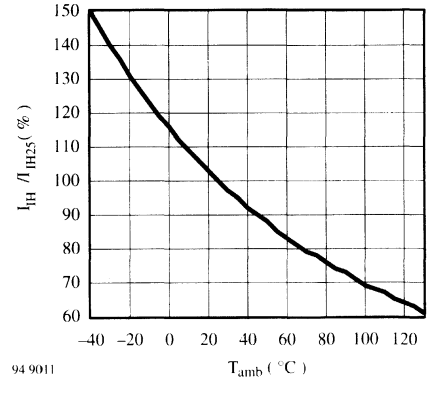


Figure 43. Input HIGH current standardized to 25°C vs. temperature

4.4 Schmitt-Trigger Inputs

The following figures show the Schmitt-trigger input specs used at timer inputs TA, TB and interrupt inputs.

Note: The values for switch levels are standardized to supply voltage.

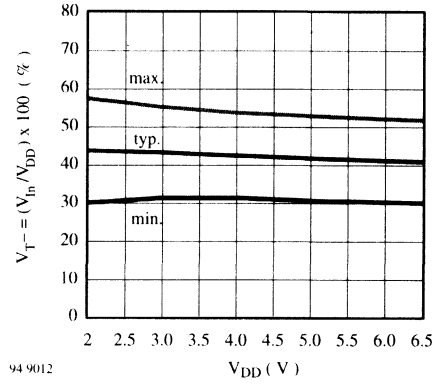


Figure 44. Schmitt-trigger positive going threshold voltage

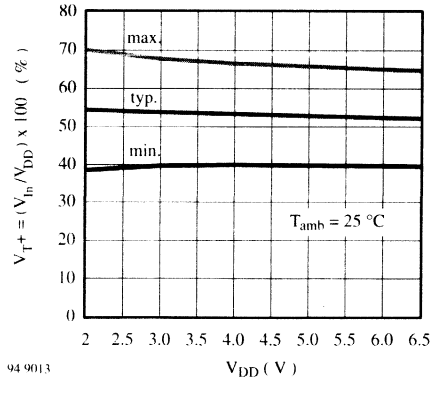


Figure 45. Schmitt-trigger negative going threshold voltage

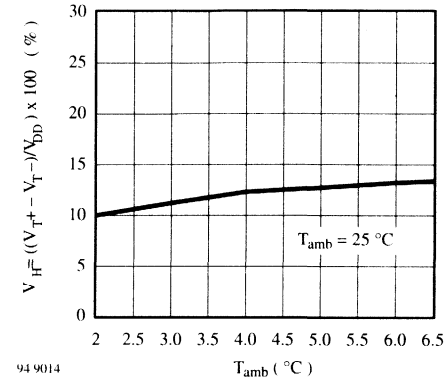


Figure 46. Schmitt-trigger hysteresis vs. supply voltage

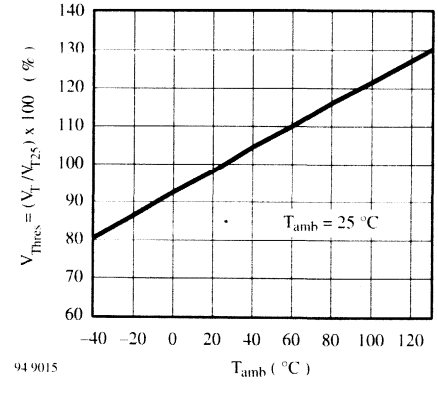


Figure 47. Threshold temperature drift

Note: For a pulse to be recognizable, it must be a minimum of 50 ns long with a rise time ≤ 10 ns.

5 Pad Layout

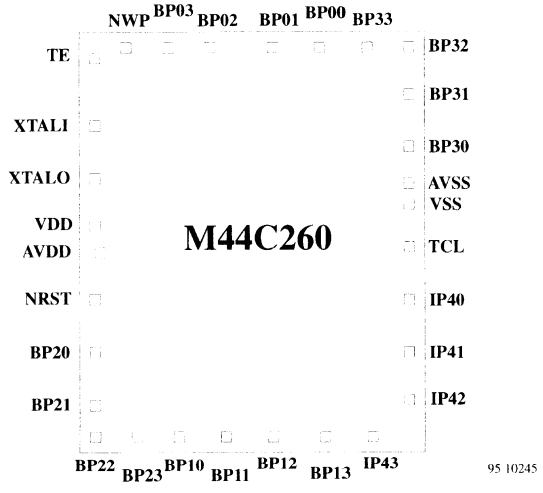


Figure 48. Pad Layout

Table 8. Pad coordinates

Number	Name	X point	Y point	Number	Name	X point	Y point
1	BP22	0,0	0,0	16	BP32	3056,0	3741,5
2	BP23	404,5	0,0	17	BP33	2651,5	3741,5
3	BP10	809,0	0,0	18	BP00	2247,0	3741,5
4	BP11	1398,5	0,0	19	BP01	1830,5	3741,5
5	BP12	1811,0	0,0	20	BP02	1136,5	3741,5
6	BP13	2223,5	0,0	21	BP03	720,0	3741,5
7	IP43	2686,5	0,0	22	NWP	303,5	3741,5
8	IP42	3056,0	509,0	23	TE	0,0	3660,0
9	IP41	3056,0	965,0	24	XTALI	0,0	3103,0
10	IP40	3056,0	1363,0	25	XTALO	0,0	2625,0
11	TCL	3056,0	1802,0	26	VDD dig.	0,0	2315,0
12	VSS	3056,0	2247,5	27	VDD ana.	24,0	2044,0
13	AVSS	3056,0	2457,5	28	NRST	0,0	1707,0
14	BP30	3056,0	3301,0	29	BP20	0,0	1164,5
15	BP31	3056,0	3741,5	30	BP21	0,0	424,5

The M44C260 is also available in the form for COB mounting. Therefore the substrate, i.e., the backside of the die, sould be connected to V_{SS}.

Die size: 3.51mm x 4.19 mm

Pad size: 90 µm * 90 µm

Thickness: 480 ± 25 µm

6 Ordering Information

Pin options

Please select the option setting from the list below.

Pin	Output		Input	
	CMOS	Open Drain	Pull Up	Pull Down
BP00				
BP01				
BP02				
BP03				
BP10				
BP11				
BP12				
BP13				
BP20				
BP21				
BP22				
BP23				
BP30				
BP31				
BP32				
BP33				
IP40–INT6				
IP41–TA				
IP42–TB				
IP43				
NWP				
TE				

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Fax: 1 708 240 –5808

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Illinois 60195
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Indiana 46248
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Bell Industries
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Indianapolis
P.O. Box 6885
Indiana 46268
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Fax: 1 317 875 –8219

Bell Industries
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Fort Wayne
Indiana 46803
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Fax: 1 219 490 –2104

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Fort Wayne
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Cedar Rapids
Iowa 52402
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Marshall Industries
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Lenexa
Kansas 66214
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Fax: 1 913 492 –6205

Hamilton/Hallmark–#58
10809 Lakeview Avenue
Lenexa
Kansas 66219
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Maryland 20877
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Hamilton/Hallmark–#12
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Columbia
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Columbia
Maryland 21046
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Fax: 1 410 290 –8006

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Bell Industries
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Fax: 1 508 474 –8902

Distributors

Zeus Electronics
25 Upton Drive
Wilmington
Massachusetts 01877
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Fax: 1 508 694 -2199

Zeus Components
607 North Avenue
Wakefield
Massachusetts 01880
Tel: 1 617 246 -8200
Fax: 1 617 246 8293

Marshall Industries
33 Upton Drive
Wilmington
Massachusetts 01887
Tel: 1 508 658 -0810
Fax: 1 508 657 -5931

Hamilton/Hallmark-#18
10D Centennial Drive
Peabody
Massachusetts 01960
Tel: 1 508 532 -3701
Fax: 1 508 532 -9802

Pioneer Std.
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Lexington
Massachusetts 02173
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Fax: 1 617 863 -1547

Michigan

Hamilton/Hallmark-#66
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Novi
Michigan 40375
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Celeste Doerwald
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Livonia
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Fax: 1 313 261 -8175

Marshall Industries
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Livonia
Michigan 48150
Tel: 1 313 525 -5850
Fax: 1 313 525 -5855

Pioneer Std.
44190 Plymouth Oaks Drive
Plymouth
Michigan 48270
Tel: 1 313 416 -2157
Fax: 1 313 416 -2415

Pioneer Std.
4467 Byron Center Road
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Michigan 49509
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Fax: 1 616 534 -3922

Future Electronics Corp.
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Fax: 1 612 944 -2520

Pioneer Std.
7625 Golden Triangle Drive
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Minnesota 55447
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Fax: 1 612 559 -8321

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Earth City
Missouri 63045
Tel: 1 314 291 -5350
Fax: 1 314 770 -6363

Marshall Industries
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Earth City
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Tel: 1 314 770 -1749
Fax: 1 314 770 -1486

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271 Route 46 West,
Ste. F202-203
Fairfield
New Jersey 07004
Tel: 1 201 227 -6060
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Marshall Industries
101 Fairfield Road
Fairfield
New Jersey 07006
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Pioneer Std.
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Fax: 1 609 596 -4266

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Tel: 1 609 234 -9100
Fax: 1 609 778 -1819

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7801 Academy Road
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New Mexico 87109-3147
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11728 Linn North East
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Fax: 1 505 275 -2819

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Port Chester
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Fax: 1 516 434 -7419

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New York 13760
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Fax: 1 607 785 –5546

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Fax: 1 716 381 –5955

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Fax: 1 716 475 –9119

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Rochester
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Fax: 1 919 878 –8729

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Fax: 1 216 248 –2312

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Fax: 1 513 898 –9835

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4433 Interpoint Blvd.
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Ohio 45424
Tel: 1 513 236 –9900
Fax: 1 513 236 –8133

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Fax: 1 513 291 –9060

Bell Industries
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Dayton
Ohio 45459
Tel: 1 513 434 –8231
Fax: 1 513 434 –8103

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Fax: 1 503 520 –1948

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Oregon 97005
Tel: 1 503 526 –6200
Fax: 1 503 641 –5939

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Oregon 97005
Tel: 1 503 644 –5050
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Fax: 1 412 963 –8255

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213 Executive Drive, Ste. 320
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Fax: 1 412 772 –1890

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Fax: 1 215 674 –3107

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Pennsylvania 19053
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Fax: 1 215 364 –4927

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Carrollton
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Fax: 1 214 447 –2222

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Texas 75081
Tel: 1 214 705 -0604
Fax: 1 214 705 -0675

Zeus Components
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Fax: 1 214 234 -4385

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Fax: 1 214 490 -6419

Marshall Industries
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Texas 77043
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Fax: 1 713 467 -9805

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Fax: 1 713 953 -8420

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Ste. 970
Houston
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Fax: 1 713 785 -4558

Pioneer Std.
10530 Rockley Road, Ste. 100
Houston
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Tel: 1 713 495 -4700
Fax: 1 713 495 -5642

Hamilton/Hallmark-#26
12211 Technology Blvd.
Austin
Texas 78727
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Pioneer Std.
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Austin
Texas 78758
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Fax: 1 512 835 -9829

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North
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Fax: 1 512 502 -0740

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84119-1552 Salt Lake City
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Bell Industries
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Utah 84047
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Fax: 1 801 255 -2477

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Tel: 1 801 467 -4448
Fax: 1 801 467 -3604

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Utah 84121
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Bellevue
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Fax: 1 206 646 -8559

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Tel: 1 206 867 -5410
Fax: 1 206 867 -5159

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Redmond
Washington 98052
Tel: 1 206 881 -6697

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Wisconsin

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Wisconsin 53146
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Fax: 1 414 780 -7201

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Marsh Electronics, Inc.
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1695 Boundary Road
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Future Electronics Corp.
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5935 Airport Road, Ste. 200
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151 Superior Blvd.
L5T 2L1 Mississauga
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Tel: 1 905 564 –6060
Fax: 1 905 564 –6033

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L4V 1X5 Mississauga
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Tel: 1 905 612 –1771
Fax: 1 905 612 –1988

Future Electronics Corp.
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1050 Baxter Road
K2C 3P2 Ottawa
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Tel: 1 613 820 –8313
Fax: 1 613 820 –3271

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Future
237 Hymus Blvd.
H9R 5C7 Pointe Claire
Quebec
Tel: 1 514 694 –7710
Fax: 1 514 695 –3707

Marshall Industries
148 Brunswick Blvd.
H9R 5P7 Pointe Claire
Quebec
Tel: 1 514 694 –8142
Fax: 1 514 694 –6989

Future Electronics Corp.
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Parana 751/55
1017 Buenos Aires
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Fax: 54 1 32 58 68 9

Electrocomponentes S.A.
Solis 225/227/229
1078 Buenos Aires
Tel: 54 1 47 61 86 4
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Brasil

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Rua Manoel Ignacio Moreira
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13210–770 Jundiai–SP
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Rua Loefgreen 1260/64
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Tel: 55 11 574 –0404
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Africa / Middle East

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Tritech Ltd
4, Hayetzira Street
43100 RA'ANANA
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Fax: 972 9 98 2 –616

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Elec Telec
Complexe Reda
9, rue Mellilia
Rabat
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South Africa

Electrolink (PTY) Ltd
Fleetway House
Martin Hammerschlag Way
Cape Town 8000
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Tunisia

Teletek
63, avenue H. Bourguiba
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Asia Pacific / Japan

Australia

IRH Components
1–5 Carter Street
2141 Lidcombe
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Tel: 61 2 36 4 –1766
Fax: 61 2 64 8 –3505

Hong Kong

Array Electronics Ltd.
Willas – Array (Holdings) Ltd.
Unit 1,24/F,
Wyler Centre Phase 2
Kowloon
Kwai Chung, N.T.
Tel: 852 2 418 –3700
Fax: 852 2 481 –6992

Audio Mechanical Corp. Ltd.
Suite 1701 A
World Finance Centre
17, Canton Road, Tsimshatsui
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Fax: 852 2 73 5 –0926

Koalink Trading Company
(Eurosil only)
39 Healthy Street East
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India

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Veer Savarkar Marg
400025 Prabhadevi, Bombay
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